Abstract

A forward silicon vertex detector (the FVTX) was developed to provide the PHENIX experiment at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory (BNL) with precise charged particle tracking at forward and backward rapidity. The requirements that the detector had to meet included (1) ability to track charged particles to a precision of 25 μm in the azimuthal direction and project those particles to a track vertex with the precision of ~100-200 μm (2) noise levels of ~500 electrons or less (3) very low mass detector configuration so that particles traversing the detector are not scattered by material (4) ability to efficiently reconstruct tracks in an environment where the occupancy of the 1-million channel detector reaches a few % (5) radiation-hard electronics in the interaction region where the detector resides.

The FVTX, half of which is shown in Figure 1, is composed of two annular endcaps, each with four stations of silicon mini-strip sensors, covering forward angles of 10°-35° (with respect to the beam line). Each station consists of 48 individual silicon sensors, which contain two columns of mini-strips with 75μm pitch in the radial direction and lengths in the azimuthal ϕ direction varying from 3.4 mm at the inner radius to 11.5 mm at the outer radius. The FVTX has approximately 0.54 million strips in each endcap. These are read out with FPHX chips, developed in collaboration with Fermilab, which are wire bonded directly to the mini-strips.

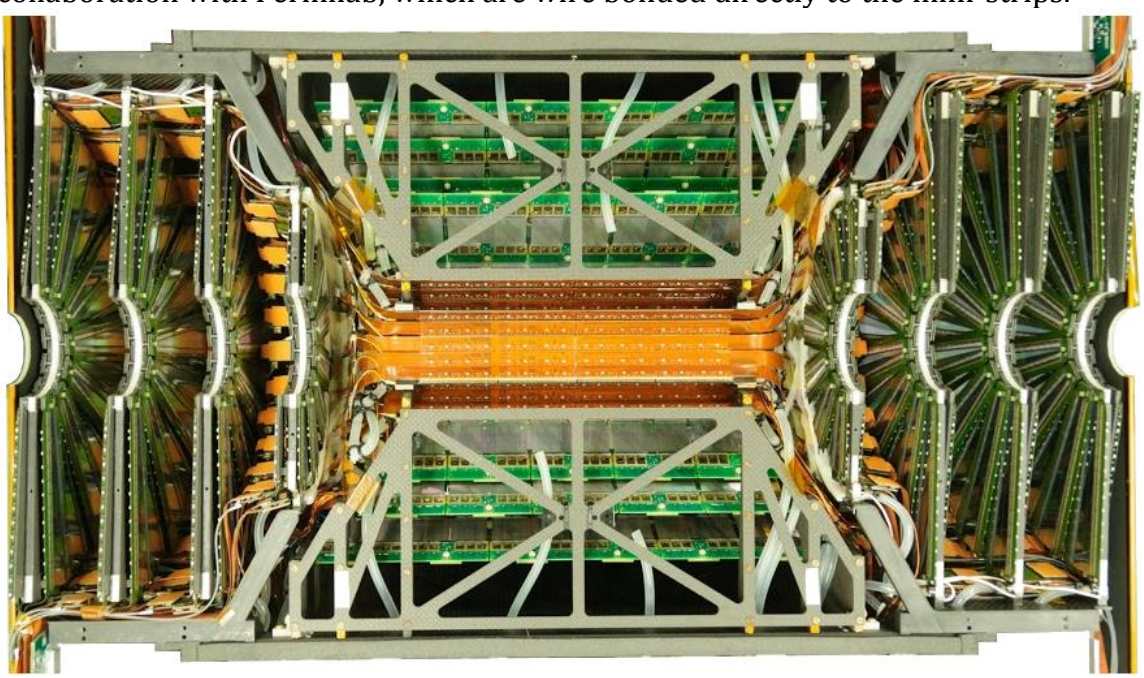

Figure 1 A photo of one-half of the FVTX detector showing a split-view of the two endcaps, one on the left and one on the right.

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Overview

Figure 2 shows a model of two quadrants of the detector, with one FVTX quadrant displaced in z for clarity. These two assembled quadrants mate with the other half of the detector around the RHIC beam pipe, which is located in the center of the detector when it is installed at RHIC. The wedges, mounted on support disks, are shown installed into their cages. A central silicon tracker (VTX) and its associated electronics are shown in the middle, mounted in the support frame. As can be seen in the figure, each cage has one small and three large disks. The smaller disks are simply truncated versions of the larger disks. A summary of the FVTX design parameters is given in Table 1.

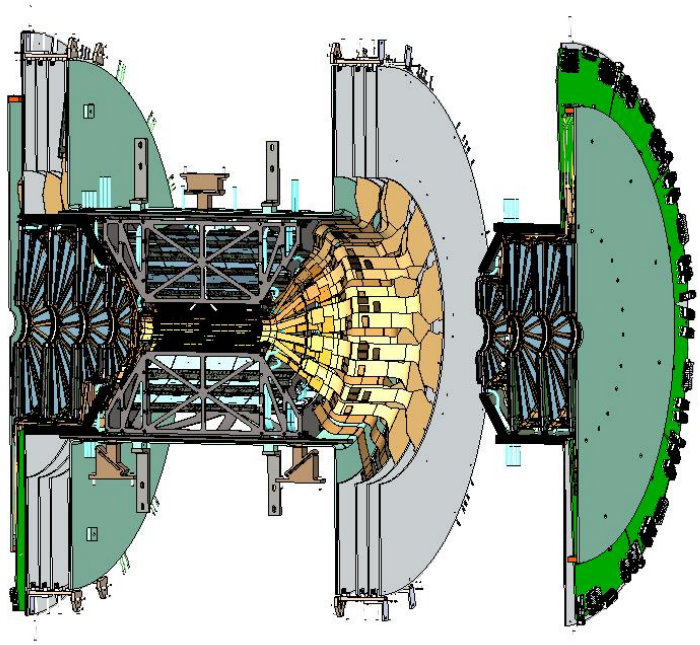

Figure 2 A drawing of the combined VTX/FVTX assembly. One FVTZ quadrant is displaced for clarity.

Silicon sensor thickness (μm)	320
Strip pitch (μm)	75
Nominal operating sensor bias (V)	70
Strips per column for small, large wedges	640, 1664
Inner radius of silicon (mm)	44.0
Strip columns per half-disk (2 per wedge)	48
Mean z-position of stations (mm)	±201.1, ±261.4, ±321.7, ±382.0
Silicon mean z offsets from station center (mm)	±5.845, ±9.845

Table 1 Summary of design parameters

Electronics:

Sensors

The silicon mini-strip sensors were designed at Los Alamos and fabricated by Hamamatsu Photonics KK. The wedge-shaped geometry comprises two individual columns of strips that are mirror images about the center line on the same sensor. The wire bond connections between the strips and read-out chips are located along the outer edges of the sensor (see Figure 3). The centerline gap between columns is 100 μm and is completely active.

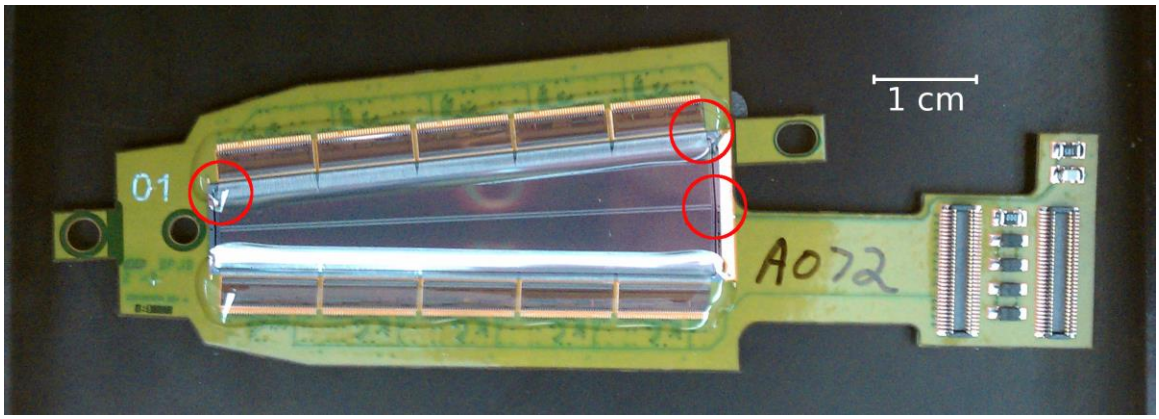

Figure 3 A completed FVTX small wedge, with sensor facing up. Note the center line dividing the two halves of the sensor and rows of FPHX chips along the sensor edges.

The strip length increases with radius on the sensor, and goes from 3.4 mm at the inner radius to 11.5 mm at the outer radius, with a pitch of 75 μm in the radial direction. Each sensor covers 7.5° in azimuthal phi, and since the strips are perpendicular to the radius, they make an angle of 86.25°.

The sensors were fabricated with p-implants on a 320 μm thick n-type substrate. The strips are AC-coupled and biased through individual 1.5 MΩ polysilicon resistors to a typical operating voltage of +70 V. The metallization on the strips is wider than the implant to provide field plate protection against micro-discharges, a concern that becomes greater with radiation-induced increases in the leakage current. The strips are also protected by two p-implant guard rings and an n^+ surround between the guard rings and sensor edge. There are two sets of bond pads for each strip, one of which is dedicated to probe tests. Each strip also has a spy pad, which is an opening through the capacitor oxide layer, that allows the DC characteristics of the strip to be probed.

FPHX Readout Chip

A custom 128-channel front-end ASIC, the FPHX, was designed by Fermilab for the FVTX detector \cite{FPHX, FPHX_JonK} with many of the setup parameters of the

front end are programmable via an LVDS serial slow control line. The chip was optimized for fast trigger capability, a trigger-less data push architecture, and low power consumption. The chip was fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) with 0.25 μm CMOS technology. The analog section consists of an integrator/shaper stage followed by a three-bit ADC.

The FPHX chip was designed to process up to four hits within four RHIC beam crossings (or ~4 times 106 ns = 424 ns). Each hit contains a 7-bit time stamp, 7-bit channel identifier, and a three-bit ADC value. By only accepting hits above a certain (programmable) ADC threshold, the signal-to-noise ratio can be dynamically optimized for different operating conditions. In addition, the ADC information from strips in an FVTX hit cluster is used to determine the center of the track via a weighted average of the charge in each strip. The data words are output over two LVDS serial lines at up to 200~MHz clock rate. The total power consumption of the FPHX is ~390 μW per channel. The noise, when the chip was wire bonded to a sensor with strips ~2—11 mm in length (~1-2.5 pF) was simulated and measured to be below the design specification of 500 electrons.

High-Density Interconnects and Extension Cables

The silicon sensor and FPHX read-out chips are assembled on a high-density interconnect (HDI) cable, which provides the slow control, power, and bias input lines as well as slow control and data output lines. The HDI stack-up is shown in Figure 4 and consists of seven layers of single- sided (20μm) and double-sided (50 μm) copper coated polyamide bonded together with a 25 μm sheet adhesive for a total thickness of approximately 350 μm. Indicated on the HDI stack-up are two signal layers, one ground layer, and one power layer. All control lines (which are not active during data taking) are routed under the sensor, and all output lines are routed towards the edge of the wedge, thus minimizing the coupling between the output lines and the sensor. The number of lines (8 pairs for the control lines and 2 signal pairs per chip for the output lines) requires that they have a 40 μm width with a 100 μm spacing. Both simulated and physical tests were carried out to ensure that the input clock (200 MHz) had sufficient integrity at the furthest point from the drive

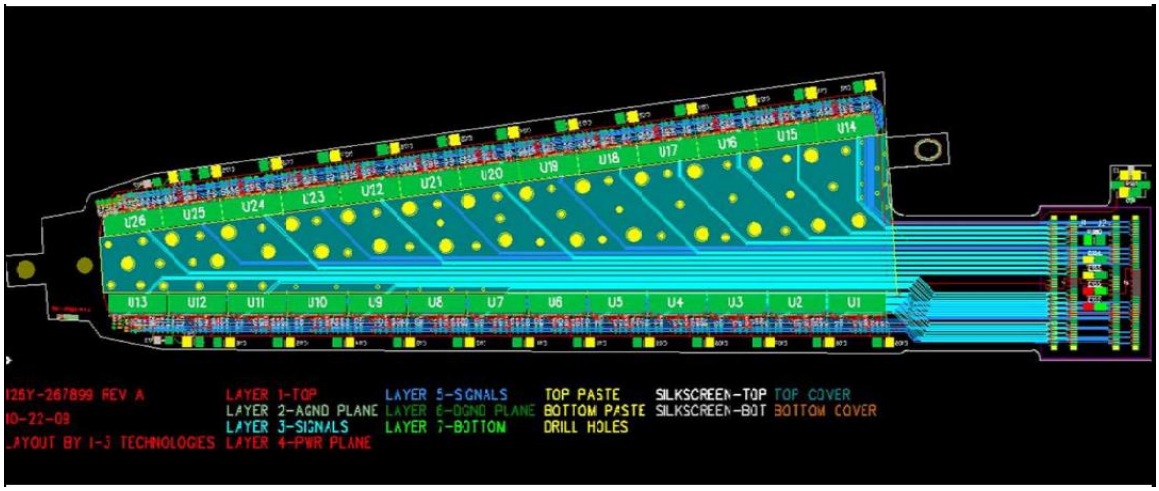

Figure 4 Schematic of the HDI stack-up.

Since the layout of the wedge, chip, and HDI can impact the system noise, the electrical layout of the wedge assembly was designed to minimize any additional noise. Incorporated onto the HDI were two noise-canceling loops, one for the input side and one for the output side of the chip, employing bypass capacitors connected to the bias ground and digital ground, respectively. Termination resistors for the calibration lines and bias resistors and capacitors are also located on the board. All elements are surface mounted and assembled by the manufacturer (Dyconex and Micro Systems Engineering).

The extension cables were designed to bring all signals from the HDI to the ROC board and power from the ROC board to the wedge, and have a similar stack-up design to the HDIs. Both the HDI and the extension cables needed to be permanently bent in multiple directions in order to precisely fit them within the constraints of the detector envelope. Bending was accomplished using fixtures which bent the flex circuits and heated them at 100° C for ~5 minutes, in order to introduce a permanent deformation.

Readout Cards/Front-End Modules

The design of the read-out electronics for the FVTX detectors is based on three major constraints, imposed by the detector:

- Large instantaneous bandwidth (3.38 Tb/s)
- Radiation hardness of read-out components near the interaction point
- Large number of I/O lines (21,000 LVDS pairs)

As a result, the read-out electronics are logically divided into two independent blocks, illustrated in Figure 5. The components are:

- **Read Out Card (ROC)** – readout module located close to the detector.
- **Front End Module (FEM)** - module which is located in the Counting House (~50 m from the Interaction Region) in a standard VME crate.
- **FEM Interface Board** - module located in each of the FEM VME crates.

The output of the FEM connects to the standard PHENIX DAQ board, a Data Collection Module (DCM), and from this point on the data stream becomes a part of the standard PHENIX DAQ.

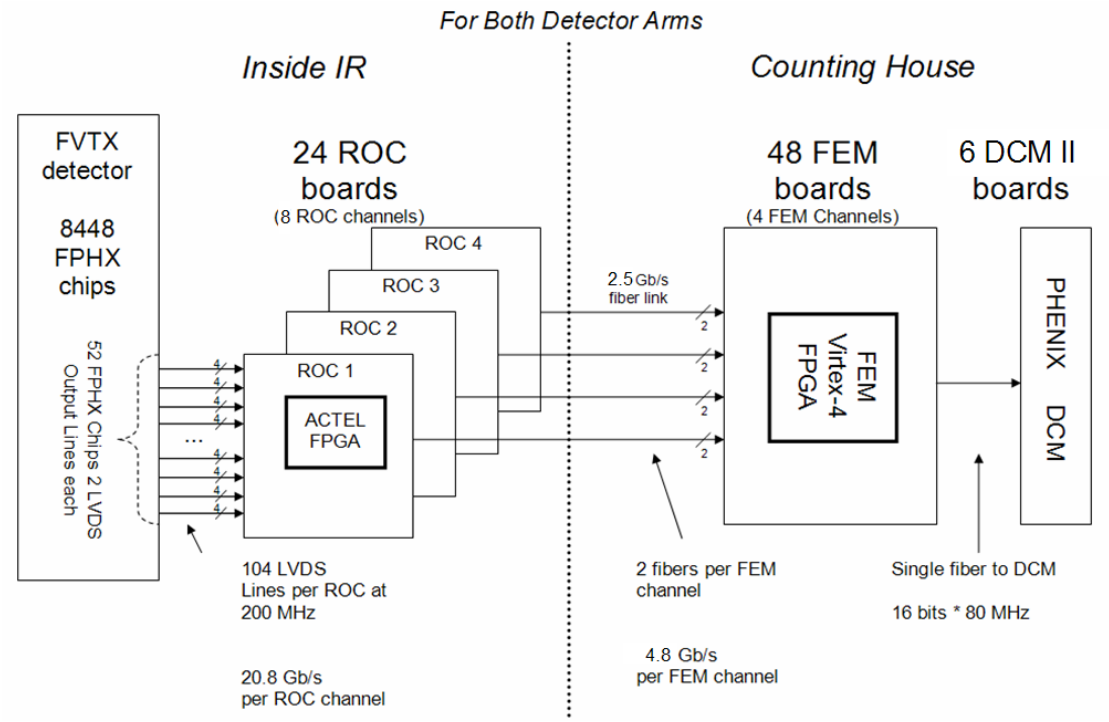

Figure 5 Read-out electronics block diagram.

The ROC for the FVTX detector were the most challenging boards to design and had to provide a number of functions for the FVTX detector including: (1) management of 1050 differential pairs of data lines from our detector, operating at 10, 105, 125, and 200 MHz (2) interfaces needed for six field programmable gate arrays (FPGAs) to perform data handling on the board (3) operation of 36 fiber optic chains running at > 1 Gbps (4) an analog calibration system with digital control which was used to calibrate 45,000 detector channels per board (1 million channels for the full system) (5) distribution of analog, digital and bias power to our silicon detectors and (6) slow control communication between a remote counting house and our on-detector electronics, as well as communication to portions of the ROC board itself. All of this operation was contained on a board constrained in physical dimension by the space available in the PHENIX detector. The electronics also had to operate in a magnetic field, in the presence of numerous other PHENIX detector electronics, and in a

radiation environment. The ROC board had to perform these functions and interface to our detector without adding to our noise specification of 500 electrons of noise. The resulting design required over 5000 components, on a 22 layer board with 5 mil trace width and spacing. The board was designed by AOT division, fabricated by DDi of Anaheim, CA and assembled by BiRa, of Albuquerque, NM. A photo of six of the assembled ROCs (12 were used for the entire system) is shown in Figure 6.

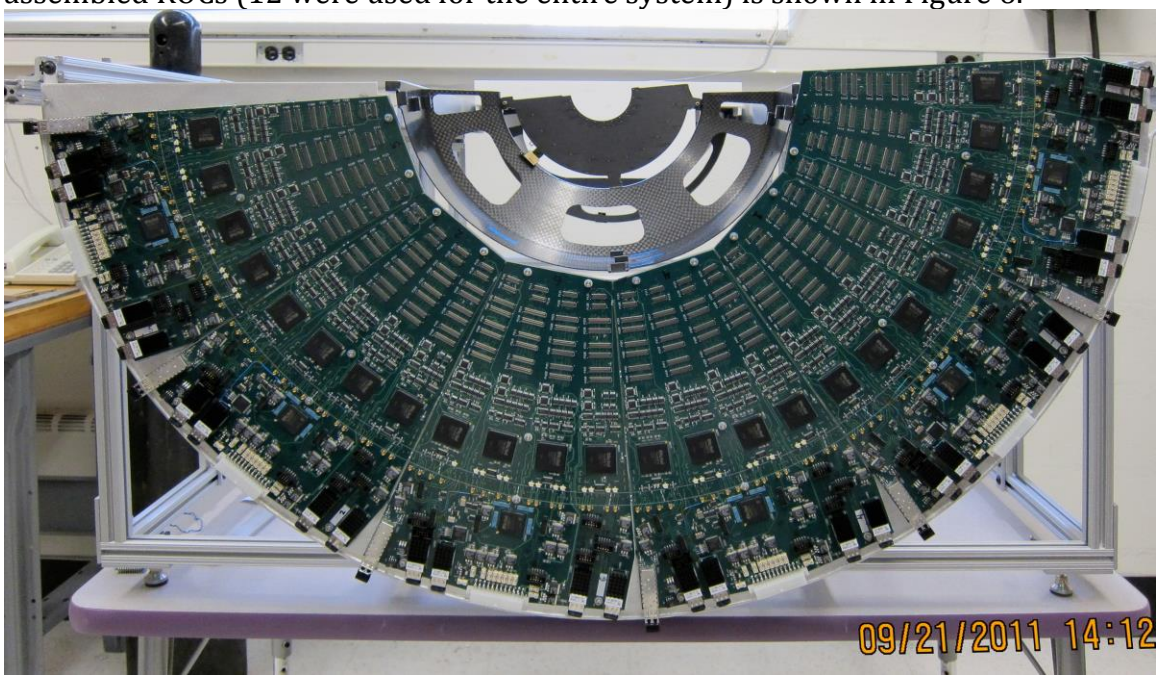

Figure 6 A photo of six of the ROCs assembled on a cooling plate and with an empty cage, which would hold four stations of FVTX wedges.

Mechanical Systems

Tight mechanical constraints plus low mass requirements resulted in the support systems for the FVTX detector to be built out of carbon-composite materials and for the cooling system to be integrated into these structures. The mechanical structures included (1) backplanes which supported the silicon sensors, FPHX readout chips and HDIs, (2) disks which formed the wedges into stations, and (3) cages which formed the stations into endcaps, all of which were fabricated by Lawrence Berkeley Laboratory. The vibrational mode frequencies, gravitational load distortions, and shape changes with temperature were studied for all mechanical structures and used to verify that the dimensional stability requirements were met.

The heat generated by the front-end readout chips was conducted from the chips to the HDI, through the wedge carbon backplane, through graphite feet to the skin of the support disks and finally to a cooling channel which was located at the outer radius of the disk. The heat generated by the ROCs was extracted from the system by mounting the ROCs onto a 1/8" aluminum plate, with 1/8" of Gap-Pad material in between to help conduct the heat and at the same time insulate the ROCs from the

conductive cooling plate. Like the disks, the ROC cooling plates also included a cooling channel at the outer radius of the plate. All cooling loops in the FVTX system used Novec 7200 (ethoxy-nanofluorobutane) as a coolant, manufactured by 3M. Novec 7200 is an engineered fluid that was developed as both a heat transfer fluid and a cleaning fluid. It is clear, non-conductive, non-corrosive, low odor and a low toxicity fluid that has zero ozone –depletion potential. The coolant leaves no residue behind when it evaporates.

Design Challenges

Some of the largest challenges encountered in the design of the FVTX detector included (1) fabrication of the HDIs and extension cables, which pushed the state-of-the art technology capabilities with the 40 μm traces spaced at 100 μm and distributed over seven layers (2) design and layout of the ROC card which resulted in a 22 layer board with high density 5-mil traces (3) development of all the FPGA codes required for the ROCs, FEMs and FEM Interface Cards which required continued refinement through the first two years of operation and (4) fabrication of the many carbon composite structures used in the system which were all produced within specs but took more time and funds to produce than were initially estimated.

Operation Challenges

One of the largest operation challenges we encountered was learning how to properly use the Novec coolant in our systems. Although the coolant has some very attractive attributes, including its non-conductive nature, which removes worries of leaks around operating electronics, we did encounter several problems with charge build-up in the system, associated with the Novec. The cooling system was comprised of a combination of aluminum, Tygon and PTFE tubes and over time it was found that the plastic tubings which we interfaced to near the detector would develop a charge build-up which would eventually discharge through the nearest conductive path. This resulted in pin-hole leaks in the tubes, and also issues with operating electronics when the closest path involved a ground path which was part of the electronics systems. The solution for our system was to replace the plastic tubing with aluminum tubing wherever possible, and we also investigated the possibility of adding a small amount of

Performance

All of the design specifications for the FVTX detector have been met since the first year of operation including (1) better than 95% efficiency for the live cannels (2) ~25 μm resolution per readout plane and (3) ~500 electrons noise for all channels.

Acknowledgments

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References

A more detailed description of the FVTX detector can be found at http://www.sciencedirect.com/science/article/pii/S0168900214004124 (Nuclear Instruments and Methods in Physics Research A, Vol 755, 11 August 2014, Pgs. 44-61.)