Front-End ASIC for a Liquid Argon TPC

Gianluigi De Geronimo, Alessio D'Andragora, Shaorui Li, Neena Nambiar, Sergio Rescia, Emerson Vernon, Hucheng Chen, Francesco Lanni, Don Makowiecki, Veljko Radeka, Craig Thorn, and Bo Yu

***Abstract*—We present a front-end application-specific integrated circuit (ASIC) for a wire based time-projection-chamber (TPC) operating in liquid Argon (LAr). The LAr TPC will be used for long baseline neutrino oscillation experiments. The ASIC must provide a low-noise readout of the signals induced on the TPC wires, digitization of those signals at 2 MSamples/s, compression, buffering and multiplexing. A resolution of better than 1000 rms electrons at 200 pF input capacitance for an input range of 300 fC is required, along with low power and operation in LAr (at 87 K). We include the characterization of a commercial technology for operation in the cryogenic environment and the first experimental results on the analog front end. The results demonstrate that complementary metal–oxide semiconductor transistors have lower noise and much improved dc characteristics at LAr temperature. Finally, we introduce the concept of "1/f equivalent" to model the low-frequency component of the noise spectral density, for use in the input metal–oxide semiconductor field-effect transistor optimization.**

***Index Terms*— Analog-to-digital converter (ADC), application-specific integrated circuit (ASIC), cryogenic, noise.**

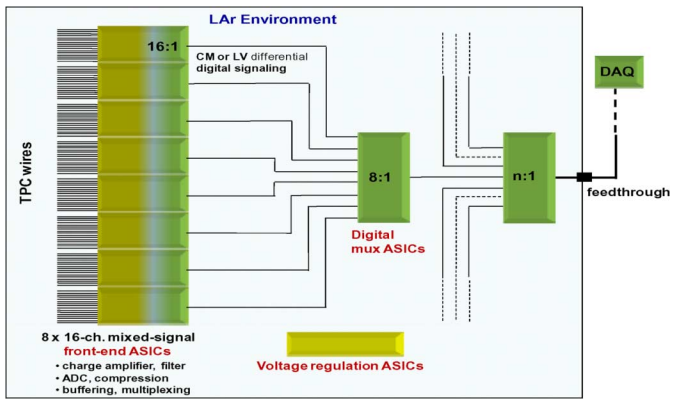

Fig. 1. Block diagram illustrating the architecture of the readout electronics for the LAr TPC. The ASICs must operate at LAr temperature (87 K), in close proximity to the ends of the detecting wires.

I. Introduction

THE LONG Baseline Neutrino Experiment (LBNE) [1], [2] aims at employing the high-power neutrino beams produced by the main injector accelerator at Fermi National Laboratory to explore neutrino oscillations, interactions, and transformations. The experimental hall will be located about 1000 km away at the site of the Homestake Mine, SD. The proposed detector will be composed of one or more 20 kton cryostats, each with size $70 \times 15 \times 15$ m^3. The modular electrode design of the wire-based Liquid Argon (LAr) time projection chamber (TPC) is described in [3]. In each wire frame module, the wires are grouped in three coplanar layers [4]. An electric field is applied in the ($\sim$2.5 m) drift space between the cathode and the readout planes, and the electrons generated by the ionizing tracks drift toward the readout wires. The first two wire planes are biased so that the electrons pass between the wires and are collected on the third plane. The first two wire planes, oriented at some angle with respect to the collecting wires, observe induced bipolar current signals and no net charge. The total number of wires in each module is on the order of 600 000, and the length and capacitance of each wire can approach, respectively, 10 m and 200 pF. For each wire, the front-end channel must read out charge signals up to 300 fC with a resolution of better than 1000 rms electrons, must digitize with 12-bit resolution at a rate of 2 MSamples/s (MS/s), and must compress, buffer, and multiplex the data to reduce the number of module feedthrough pins to a few thousands. The power dissipated by each channel must be constrained within $\sim$10 mW.

Fig. 1 shows the architecture of the LAr TPC readout electronics, submerged in liquid Argon (i.e., at 87 K), and composed of front-end mixed-signal application-specific integrated circuits (ASICs) (providing charge amplification, analog processing, digitization, compression, and a first 16:1 multiplexing), one or more digital multiplexing ASICs, and voltage regulation ASICs.

In this paper, we discuss the development of the front-end mixed-signal ASIC. In Section II, we report on the characterization of the 180 nm CMOS technology selected for the initial development, with particular attention focused on the performance in the cryogenic environment. We also introduce the concept of "1/f equivalent" and discuss the input MOSFET optimization for LAr TPC. In Section III, we present the ASIC architecture, we describe the first prototype of analog front end, which was developed using the original foundry models and parameters, we report on the first experimental results, and we introduce the 12-bit analog-to-digital converter (ADC), which will be fabricated as a separate ASIC in the development phase.

II. Cryogenic CMOS

With a wire capacitance approaching 200 pF, a resolution of better than 1000 rms electrons can only be achieved if the front-end electronics are located in close proximity to the wire

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G. De Geronimo, S. Li, N. Nambiar, S. Rescia, E. Vernon, H. Chen, F. Lanni, D. Makowiecki, V. Radeka, C. Thorn, and B. Yu are with the Brookhaven National Laboratory, Upton, NY 11973-5000 USA (e-mail: degeronimo@bnl.gov).

A. D'Andragora is with the University of L'Aquila, L'Aquila 67100, Italy.

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ends (i.e., in the liquid Argon (87 K)). Moving the front end outside the cryogenic environment (300 K) would require, along with the additional meters of interconnect (increased capacitance and noise), a prohibitive number of feedthroughs (one or two for each of the ∼600 000 wires). It would also make the cryostat design more complex.

In operating the CMOS technologies at the cryogenic temperature of 87 K, two critical aspects must be considered: 1) the reliability of the device models in terms of the ASIC operating point, signal response (transconductance, output resistance, and capacitance), noise, and passive components (linear resistors and capacitors), and 2) the lifetime, considering that the LAr TPC is required to operate for more than 20 years with limited access to the electronics for repair or replacement. We will report here on the former; while the latter, still being studied, will be briefly discussed at the end of this section.

As shown in Section III, we designed, fabricated, and characterized, in a commercial 180 nm CMOS technology, an analog front-end ASIC. For this first prototype, we adopted the CMOS models and parameters for room temperature provided by the foundry, and just assumed some model reliability when simulating at the cryogenic temperatures of interest. This assumption was, in part, justified by our results on the characterization of a mixed-signal 250 nm CMOS ASIC, originally developed for room temperature applications [5], and tested at temperatures down to 40 K [6]. The signal and noise responses were, to a first order, in agreement with the simulations. Along with the design of a complete analog front end, we integrated a number of test structures. In this section, we discuss the results of this characterization, which was performed at 300 K and 77 K (i.e. fully submerged in liquid nitrogen). The technology is the 180 nm CMOS from TSMC.

A. DC Characteristics

Fig. 2 shows the comparison between the simulated and measured dc characteristics of an n-channel MOSFET with a gate length $\mathrm{L} = 180$ nm and a gate width $\mathrm{W} = 10\ \mu$m (five 2-μm fingers). Very good agreement can be observed at room temperature, while some difference in the saturation voltage, subthreshold slope, and transconductance can be observed at 77 K. In Fig. 2, the subthreshold slope is expressed by using its inverse (change in gate voltage per decade of drain current), and it approaches an expected $\mathrm{ln}(10)\mathrm{nV_t}$ [7], where $\mathrm{n} \approx 1.3$ is the subthreshold slope factor, and $\mathrm{V_t} = \mathrm{k_B T/q}$ is the thermal voltage. These results are in good agreement with others reported in the literature [8]–[10].

As discussed in Section III, the impact of these differences on the performance of our first ASIC prototype was small. However, we will consider modifying the model parameters in the next revision to better approximate the actual curves.

Results from the literature [9]–[12] indicate negligible dependence of the MOSFET capacitive components on the temperature. Fig. 3(a) shows the simulated dependence of the total gate capacitance on the drain current density for n- and p-channel MOSFETs at different channel lengths. For a given device, a shift in the rising edge at about three times the current density can be observed from 300 K to 77 K. The center of moderate inversion (where the inversion coefficient integrated circuit (IC)

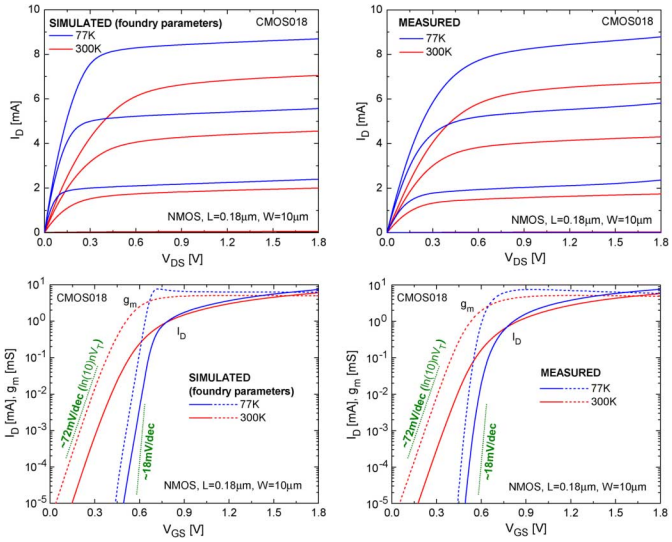

Fig. 2. Simulated (left) and measured (right) dc characteristics of an n-channel MOSFET with $\mathrm{L} = 180$ nm at 300 K (red curves) and 77 K (blue curves).

is equal to unity), which occurs at the center of the rising edge, shifts with the same factor ∼3. The inversion coefficient IC, as derived from the EKV model [13]–[16], can be expressed as

$$\mathrm{IC} = \frac{\mathrm{I_D}}{2\mathrm{n}\,\mu(\mathrm{T})\,\mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}\mathrm{V_t^2}} \tag{1}$$

where $\mathrm{C_{ox}}$ is the gate–oxide capacitance per unit area and μ is the charge mobility, which depends on the temperature and is estimated to increase a factor ∼5 from 300 K to 77 K [11], [16]. For the selected technology $\mathrm{C_{ox}} \approx 8.4\ \mathrm{fF}/\mu\mathrm{m}^2$ and $\mu_{300\ \mathrm{K}} \approx 400$ and 83 $\mathrm{cm^2 V^{-1} s^{-1}}$ for n- and p-channel devices, respectively. From (1), it follows that, for a given drain current $\mathrm{I_D}$, the inversion coefficient increases a factor ∼3 from 300 K to 77 K. Consequently, the region of moderate inversion [14], where $0.1 < \mathrm{IC} < 10$, shifts at 77 K, about 3 times toward higher current density.

B. Noise

With regards to the noise, we approximate the equivalent input spectral density of the MOSFET with the following operative model [17], [18] (a discussion on its origin is beyond the scope of this paper)

$$\mathrm{S_V} = \frac{\mathrm{K_f(IC,L,T)}}{\mathrm{C_{ox}WLf}^{\alpha_\mathrm{f}(\mathrm{IC,L,T})}} + \alpha_\mathrm{w}(\mathrm{IC,L,T})\mathrm{n4kT}\frac{\gamma(\mathrm{IC})}{\mathrm{g_m(IC,L,T)}} \tag{2}$$

composed of a low-frequency term and a white term. In the low-frequency term, the amplitude coefficient $\mathrm{K_f}$ $(\mathrm{joule \cdot Hz}^{\alpha_\mathrm{f}-1})$ and the slope factor α_f depend on the inversion coefficient IC (i.e., on drain current density), channel length L, and temperature T. Similarly, in the white term, the noise excess coefficient α_w and the transconductance $\mathrm{g_m}$ depend on IC, L, and T. The gamma coefficient depends on the IC and can be approximated with [17]

$$\gamma = \frac{1}{1+\mathrm{IC}}\left(\frac{1}{2} + \mathrm{IC}\frac{3}{2}\right). \tag{3}$$

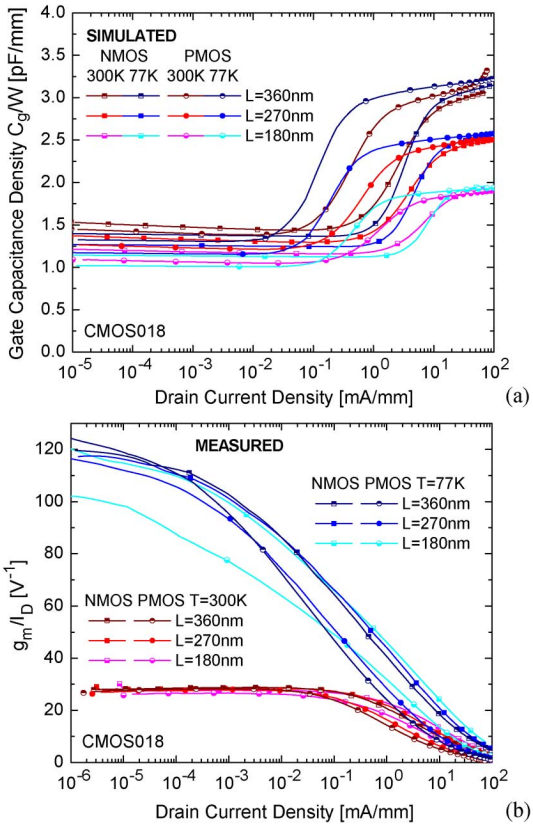

Fig. 3. Simulated total gate capacitance (a) and measured g_m/I_D ratio (b) as functions of the drain current density I_D/W. Red and blue curves are, respectively, for room (300 K) and liquid nitrogen (77 K) temperatures.

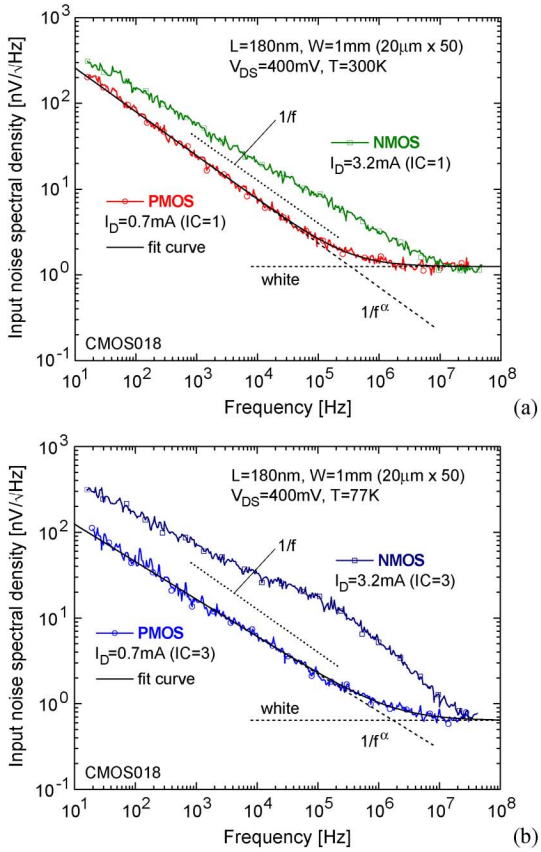

Fig. 4. Measured equivalent input noise spectral densities at 300 K (a) and 77 K (b) on n- and p-channel MOSFETs with $L = 180$ nm.

The g_m in (2) can be either simulated or extracted from the dc measurements. In Fig. 3(b), we show the measured ratio g_m/I_D as a function of the drain current density I_D/W for n- and p-channel MOSFETs with different channel lengths. It can be observed that as I_D decreases, the ratio g_m/I_D tends to the asymptotic value $(nV_t)^{-1}$ which is about 30 and 115 V^{-1} at 300 K and 77 K, respectively. Considering that the input MOSFET typically operates in moderate inversion, a g_m increase of about 2 at equal drain current I_D should be expected when operating at the cryogenic temperatures of interest. It follows that the white term in (2) is expected to decrease about 8 times (4 from the temperature coefficient T, 2 from the increase in g_m), assuming no change in α_w.

The coefficients α_w, K_f, and α_f must be extracted from measurements of the equivalent input noise spectral density. In Fig. 4(a), we show the measurements at 300 K on n- and p-channel MOSFETs with $L = 180$ nm, $W = 1$ mm, and $IC = 1$ ($I_D =$ 3.2 and 0.7 mA, respectively). While exhibiting a comparable K_f (i.e., a comparable noise at 1 Hz), the p-channel is characterized by a higher slope (higher α_f, $\sim$1.025 compared to the $\sim$0.89 of the n-channel), which makes it substantially more advantageous for low-noise applications.

The corresponding measurements at 77 K are shown in Fig. 4(b), where we biased the devices at the same drain current I_D (i.e., with $IC \approx 3$). In n-channel devices, we invariably observed an increase in the region between 10 kHz and 10 MHz, which resembles a contribution from a Lorentizan packet [19]–[21] and which made impossible the extraction of the white term. In p-channel devices, along with the expected decrease in the white term, we observed some decrease in the low-frequency component at 1 Hz (K_f from 1.084×10^{-24} to 0.175×10^{-24} J) along with a decrease in the slope (α_f from 1.025 to 0.88) so that the noise value around 100 kHz was practically comparable.

We measured the input noise spectral densities for different channel lengths and operating points (different values of drain current I_D, and drain-to-source voltage V_{DS}). Negligible dependence on V_{DS} (above saturation) was observed at a given I_D. In Fig. 5, the measurements at 300 K and 77 K on n- and p-channel MOSFETs biased at $IC = 1$ are shown, while Fig. 6 shows the measurements versus IC (i.e., versus I_D) for the case of n- and p-channel MOSFETs with $L = 270$ nm. Using a minimum square fitting algorithm on (2) in the $\sim$1 kHz to $\sim$20 MHz region, we extracted the values of α_w, K_f, and α_f given in Fig. 7.

With regards to the white noise excess coefficient α_w, we extracted values larger than unity, increasing with the drain current density (i.e., with an IC). The increase was more pronounced at shorter channel lengths and it was particularly steep in n-channel devices, presumably due to electron multiplication. These results are in agreement with several others reported in the literature. See, for example, [22] and [23], where physical models are also discussed. Concerning the measurements at 77 K, as previously discussed, it was not possible to extract the coefficient for n-channel devices, while some increase with IC was observed in p-channel devices, especially at minimum channel length.

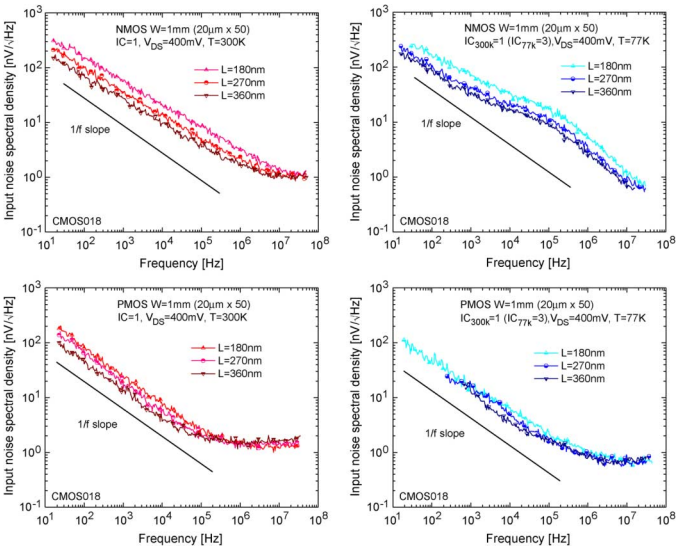

Fig. 5. Measured equivalent input noise spectral densities at 300 K (left) and 77 K (right) on n- and p-channel MOSFETs with different channel lengths and $\mathrm{IC}_{300\ \mathrm{K}} = 1$ ($\mathrm{IC}_{77\ \mathrm{K}} = 3$).

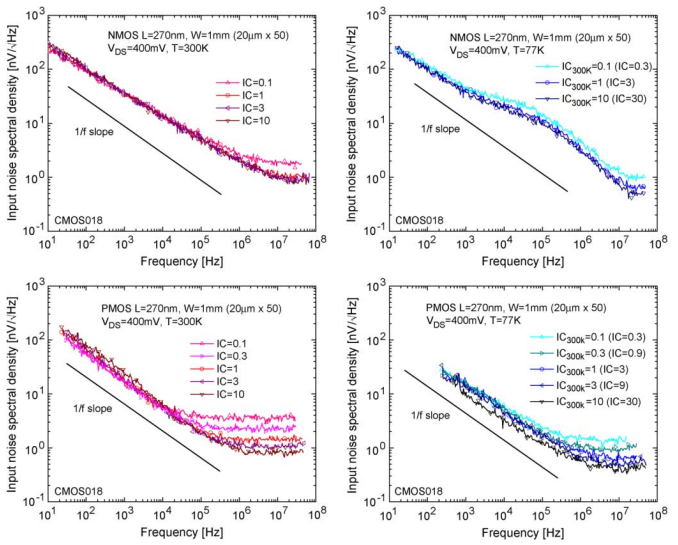

Fig. 6. Measured equivalent input noise spectral densities at 300 K (left) and 77 K (right) on n- and p-channel MOSFETs with $\mathrm{L} = 270$ nm and different drain current densities (different values of IC).

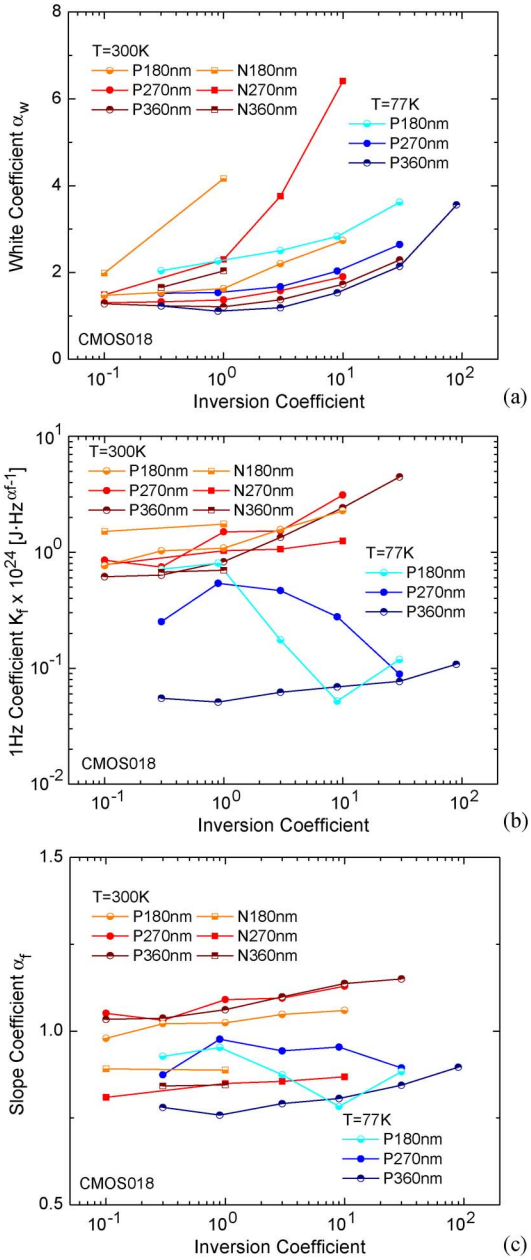

Fig. 7. (a) Noise coefficients α_{w}. (b) $\mathrm{K_f}$. (c) α_{f} for the model (2), extracted by using a minimum square fitting algorithm on (2) in the ~1 kHz to ~20 MHz from spectral measurements on n- and p-channel MOSFETs at different channel lengths and values of the inversion coefficient IC (i.e., drain current density).

With regards to the low-frequency noise coefficients, $\mathrm{K_f}$ and α_{f}, the measurements at 300 K show an increase in $\mathrm{K_f}$ with the drain current density, more pronounced in p-channel devices. This seems to be in agreement with other results reported in the literature [24]–[28]. However, the increase in $\mathrm{K_f}$ was accompanied by a corresponding increase in the slope coefficient α_{f} so that the low-frequency noise contribution in the 10 kHz to 100 kHz region was practically unchanged. Hence, the input MOSFET optimization process must consider both coefficients, as discussed later. Concerning the measurements at 77 K, the dependence of the $\mathrm{K_f}$ and α_{f} were quite irregular, especially in the case of minimum channel length. However, also in those cases a change in $\mathrm{K_f}$ was accompanied by a corresponding change in the slope coefficient α_{f}.

C. Equivalent Noise Charge

The expression for the equivalent noise charge (ENC) can be used to: 1) optimize the size and operating point of the input MOSFET and 2) estimate the achievable ENC. It can be modeled with [17]

$$\mathrm{ENC}^2 = [\mathrm{C_{in}} + \mathrm{C_{gw}}(\mathrm{IC},\mathrm{L},\mathrm{T}) \cdot \mathrm{W}]^2 \times \left[\frac{\mathrm{a_w}}{\tau_{\mathrm{p}}} \frac{\alpha_{\mathrm{w}} \mathrm{n} \gamma(\mathrm{IC}) 4\mathrm{kT}}{\mathrm{g_{mw}}(\mathrm{IC},\mathrm{L},\mathrm{T}) \cdot \mathrm{W}} + \frac{\mathrm{K}_f(\mathrm{IC},\mathrm{L},\mathrm{T})}{\mathrm{C_{ox}WL}} \times \frac{(2\pi)^{\alpha_{\mathrm{f}}(\mathrm{IC},\mathrm{L},\mathrm{T})}}{\tau_{\mathrm{p}}^{1-\alpha_{\mathrm{f}}(\mathrm{IC},\mathrm{L},\mathrm{T})}} \mathrm{a_f}\left(\alpha_{\mathrm{f}}(\mathrm{IC},\mathrm{L},\mathrm{T})\right)\right] \quad (4)$$

where $\mathrm{C_{in}}$ is the external input capacitance, which includes the sensing wire and the interconnects, and which does not scale

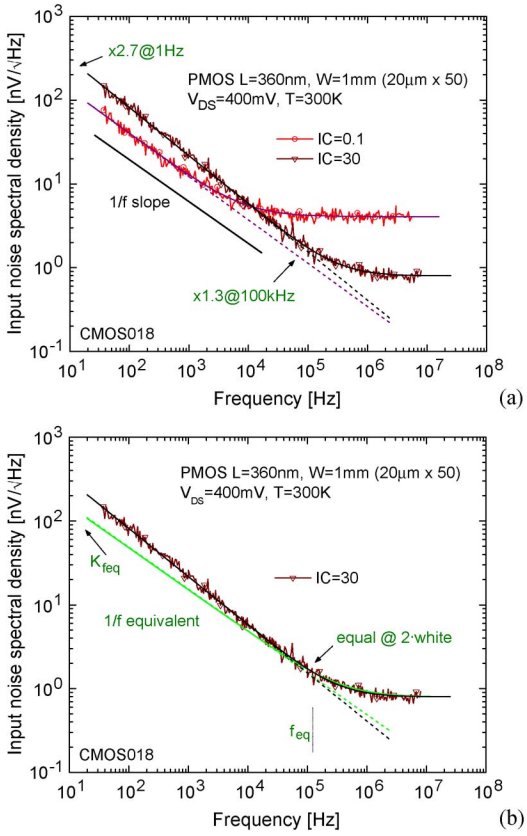

Fig. 8. (a) Comparison between noise spectral densities at $\mathrm{IC} = 0.1$ and $\mathrm{IC} = 30$ for a p-channel MOSFET with $\mathrm{L} = 360$ nm at $\mathrm{T} = 300$ K. (b) Illustration of the concept of 1/f equivalent, defined in (5) as the 1/f noise which gives a total contribution equal to the measured noise at a specific frequency $\mathrm{f_{eq}}$ where the noise is equal to twice the white noise.

with the width W of the input MOSFET (i.e., any capacitance, including the interconnect and parasitics); $\mathrm{C_{gw}}$ and $\mathrm{g_{mw}}$ are the gate capacitance and transconductance per unit of W, τ_p is the peaking time, and $\mathrm{a_w}$ and $\mathrm{a_f}$ are coefficients that depend on the type of shaping [17], [18], typically on the order of 1 and 0.5, respectively.

As can be observed from (4), the dependence of the $\mathrm{K_f}$ and α_f on the bias point can make the optimization process quite cumbersome. In the next section, we discuss an alternative and simpler approach.

D. 1/f Equivalent

In Fig. 8(a), we consider the example of a *p*-channel MOSFET with $\mathrm{L} = 360$ nm at $\mathrm{T} = 300$ K. As previously discussed, to an increase in increase $\mathrm{K_f}$ with IC corresponds an increase in α_f. For $\mathrm{IC} = 30$ it follows that while the noise at 1 Hz is about 2.7 times larger, the difference is reduced to 1.3 at 100 kHz, as shown in Fig. 8(a).

We now define "1/f equivalent" the 1/f noise which gives a total contribution equal to the measured noise at a specific frequency $\mathrm{f_{eq}}$, which is defined at the frequency where the noise density is equal to twice the white noise (a factor of four in power)

$$\mathrm{S_{veq}(f)} = \frac{\mathrm{K_{feq}}}{\mathrm{C_{ox}WLf}} + \mathrm{white}$$
$$\text{where } \mathrm{K_{feq}} = 3\mathrm{C_{ox}WLf_{eq}} \times \mathrm{white},\ \mathrm{S_v(f_{eq})} = 4 \times \mathrm{white} \quad (5)$$

and we define $\mathrm{K_{feq}}$ (Joule) as "equivalent $\mathrm{K_f}$." This concept is illustrated in Fig. 8(b) where the case $\mathrm{IC} = 30$ is approximated by using its 1/f equivalent. This choice can be justified considering that in most practical cases, the input MOSFET is biased at a current where the low-frequency noise slightly dominates on the white noise, while a further increase in current would result in an increase in power with only a marginal benefit in resolution.

Obviously, a dependence of the $\mathrm{K_{feq}}$ on the operating point must be expected. However, the dependence is modest, as can be observed from Fig. 9(a), where we plot the values of the extracted $\mathrm{K_{feq}}$. The 1/f equivalent (i.e., the $\mathrm{K_{feq}}$) can be used in the ENC equation, yielding the known

$$\mathrm{ENC}^2 = [\mathrm{C_{in}} + \mathrm{C_{gw}(IC, L, T)} \cdot \mathrm{W}]^2 \left[\frac{\mathrm{a_w}}{\tau_\mathrm{p}} \frac{\alpha_\mathrm{w} \mathrm{n} \gamma(\mathrm{IC}) 4\mathrm{kT}}{\mathrm{g_{mw}(IC, L, T)} \cdot \mathrm{W}} + 2\pi \mathrm{a_f} \frac{\mathrm{K_{feq}(IC, L, T)}}{\mathrm{C_{ox}WL}}\right] \quad (6)$$

where the expression for the low-frequency noise contribution is greatly simplified.

The impact on the MOSFET optimization process and on the ENC estimate can be appreciated from Fig. 9(b), where the ENC versus W (input MOSFET width) for $\mathrm{C_{in}} = 1$ pF and $\tau_\mathrm{p} = 1\ \mu$s is shown for three different values of dissipated power: 0.1, 1, and 10 mW (dashed, solid, and dotted curves, respectively). The curves using (4) and (6) (black and red, respectively) are close, suggesting negligible error in the optimization process (optimum W) and a small error in the estimate (minimum ENC). The cases for 0.1 mW represent a situation where the white noise contribution tends to dominate, while the ones for 10 mW are for the opposite. The value of the inversion coefficient IC is also shown at the minimum ENC, ranging from 0.5 at 0.1 mW to 30 at 10 mW. As it must be expected, the benefit in increasing the dissipated power becomes eventually negligible since the low-frequency component dominates. The difference between the curves becomes more visible only in those (rare and impractical) cases where a relatively large amount of power (i.e., a large amount of mW/pF) is available. In Fig. 9(b), the curves using an "averaged 1/f equivalent" are also shown (blue curves), where a single value $\langle \mathrm{K_{feq}} \rangle$ has been adopted, as an average value of $\mathrm{K_{keq}}$ versus IC from Fig. 9(a). Also in this more simplified case, the errors in optimization and estimate appear acceptable.

Intuitively, a large increase in dissipated power (i.e., a decrease in white noise) should move the optimum width W towards larger values, since white and 1/f noise contributions have a minimum for $\mathrm{C_g} \ll \mathrm{C_{in}}$ (typically one third when operating in strong inversion and much lower when operating in a moderate inversion [17]) and $\mathrm{C_g} \approx \mathrm{C_{in}}$, respectively. As shown in Fig. 9(b), this shift does not actually occur from 1 mW to 10 mW. This can be understood by observing Fig. 9(c) where the white and 1/f noise contributions are also reported for 1 mW and 10 mW. As expected, the white contribution decreases as the power increases, but the increase with W is somewhat steeper. More relevant, the 1/f contribution shows a large dependence on the dissipated power, becoming larger as the power increases, and with the minimum shifted towards lower values of W. This

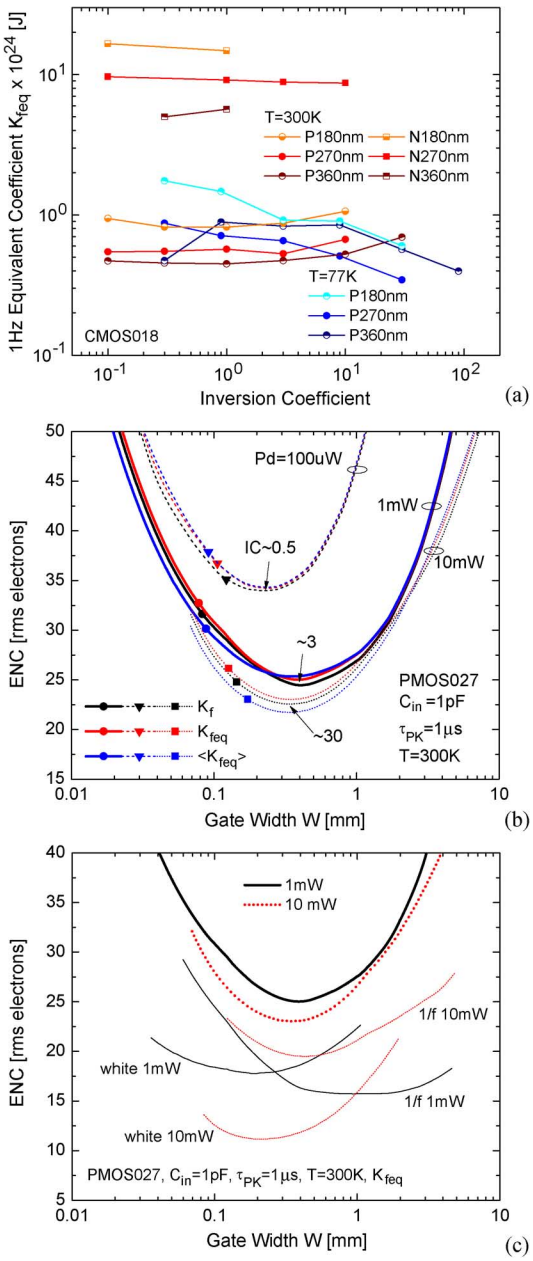

Fig. 9. (a) Plot of the coefficient $\mathrm{K_{feq}}$ defined as in (5). (b) Impact of using $\mathrm{K_{feq}}$ and its average $\langle \mathrm{K_{feq}} \rangle$ on the optimization curves ENC versus W for the case of $\mathrm{C_{in}} = 1\ \mathrm{pF}$, $\tau_{\mathrm{p}} = 1\ \mu\mathrm{s}$, and different values of dissipated power: 0.1 mW, 1 mW, and 10 mW. (c) White and 1/f contributions for the 1 mW and 10 mW cases at (b) by using $\mathrm{K_{feq}}$.

trend at large values of dissipated power is explained with the increase in the gate capacitance per unit of width W [see Fig. 3(a)].

Concerning the choice of the length L of the p-channel input MOSFET, the analysis of this technology suggests an optimum between the minimum and twice that (i.e., between 180 nm and 360 nm). For large values of milliwatts per pF, better results are achieved for L in the range 180 nm to 270 mm; for small values of milliwatts per pF, better results are achieved for L in the range of 270 nm to 360 nm. As previously discussed, the dependence of the gate capacitance per unit of width W on the drain current density plays a large role. In our case, we selected $\mathrm{L} = 270$ nm, as illustrated in the following section.

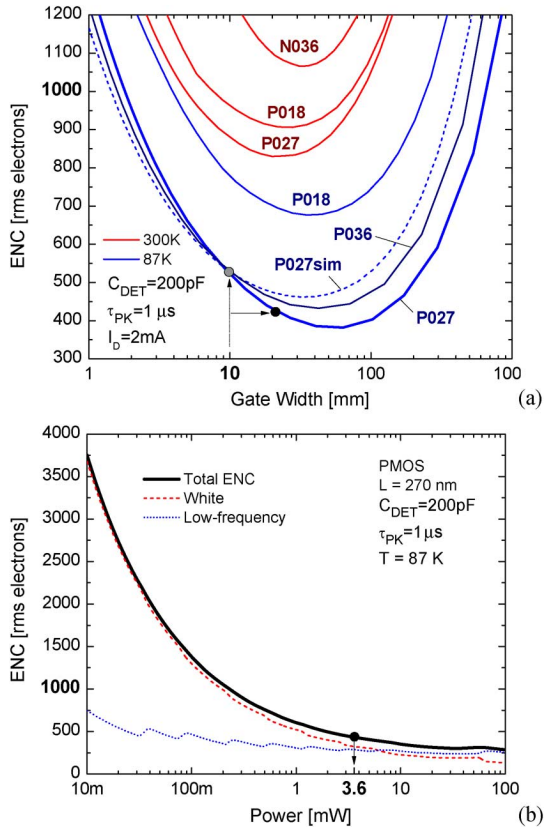

Fig. 10. (a) ENC veersus W for different MOSFETs at 300 K and 87 K. The dashed line represents our original simulations based on assumed values for the noise parameters; the solid lines are based on the measured values. (b) ENC versus dissipated power at $\mathrm{T} = 87$ K for the case of p-channel MOSFET with $\mathrm{L} = 270$ nm, with corresponding low-frequency and white contributions.

E. MOSFET Optimization for LAr TPC

The front-end electronics for our TPC must provide, when operating in liquid Argon (87 K), a resolution better than 1000 rms electrons, with an input capacitance $\mathrm{C_{in}}$ from the sensing wires as high as 200 pF [3]. Since the maximum input charge can approach 300 fC ($\sim 1.9 \times 10^6$ electrons), the required dynamic range, defined as the ratio between the maximum input charge and the ENC, must exceed 2000. This imposes a constraint on the design of the filter, which will be discussed elsewhere [29].

The input MOSFET optimization is illustrated in Fig. 10 where we show the ENC versus W for different channel lengths at 300 K and 87 K (for the latter, we approximated the values of some parameters with the ones measured at 77 K) with $\mathrm{I_D} = 2$ mA (3.6 mW) and $\tau_{\mathrm{p}} = 1\ \mu$s. The dashed line represents our original simulation, based on originally assumed values for the noise parameters, while the solid lines are based on the recently acquired measured values. We selected a gate width $\mathrm{W} = 10$ mm since, according to the original simulations, only a modest improvement (from $\sim 530\ \mathrm{e^-}$ to $\sim 480\ \mathrm{e^-}$ (i.e., $\sim 220\ \mathrm{e^-}$) was to be expected for larger values of W. On the other hand, the simulations based on the measured values now indicate a larger improvement (from $\sim$ 530 $\mathrm{e^-}$ to $\sim$ 420 $\mathrm{e^-}$ (i.e., $\sim$ 320 $\mathrm{e^-}$) if we increase W from 10 mm to 20 mm, which appears more attractive and will be implemented in the revision of the design.

The ENC versus dissipated power is shown in Fig. 10(b), along with the low-frequency and white contributions, for the case of the selected p-channel MOSFET with $\mathrm{L} = 270$ nm at $\mathrm{T} = 87$ K. We chose 3.6 mW (i.e., 2 mA), beyond which there is a diminishing return. At this operating point, the two contributions are somewhat comparable.

F. Lifetime

With regards to the lifetime, the major failure mechanisms, such as electromigration (EM), stress migration (SM), time-dependent dielectric breakdown (TDDB), and thermal cycling (TC) scale in favor of cryogenic operation [30], [31]. The only mechanism that can affect the lifetime at cryogenic temperature is the degradation due to impact ionization, which causes charge trapping in the MOSFET gate oxide [32].

A monitor of the impact ionization is the bulk current, which reaches a maximum at $\mathrm{V_{DS}} = \mathrm{V_{DD}}$ and at $\mathrm{V_{GS}} \approx 0.5\ \mathrm{V_{DD}}$. When operating constantly in this condition, the device at room temperature has a lifetime (defined as a 10% degradation in $\mathrm{g_m}$) of about 10 years. The bulk current (i.e., the impact ionization) increases roughly a factor four at 77 K with respect to 300 K [32]. In order to guarantee the required lifetime, different design guidelines must be adopted for analog and digital circuits. The former case consists of operating the devices at moderate-to-low drain current densities, where the impact ionization is negligible. The latter case consists of operating the devices with reduced $\mathrm{V_{DD}}$ (about 20%) and adopting nonminimum channel length L, considering that at cryogenic temperature, the speed of the digital circuit [33] increases, thus compensating for the increased L. We will verify these guidelines with accelerated aging tests on dedicated structures and will report the results in a future publication.

III. ASIC Architecture and Analog Front End

In Fig. 11, we show a block diagram of the proposed 16-channel front-end ASIC. Each channel includes a charge amplifier with adjustable gain (4.7, 7.8, 14, and 25 mV/fC, to cover, respectively, a range of 55, 100, 180, and 300 fC), a high-order antialiasing filter with an adjustable time constant (peaking time 0.5, 1, 2, 3 μs), option to enable an ac coupling stage, baseline adjustment to 200 mV or 900 mV for operation with either the collecting or the noncollecting wires, a 12-bit 2 MSamples/s ADC, and a data compression stage.

Shared among the 16 channels are the bias circuits, registers, a temperature monitor, a pulse generator, the digital multiplexer, an analog buffer for signal monitor, and the digital interface. A 600 kbit buffer will be integrated, capable of storing up to 1.5 ms worth of event, sampled at 2 MSamples/s, in each channel and assuming no compression. Two or more events can be stored with compression. The projected layout size, pads included, is on the order of 11×6 mm^2. The expected dissipated power is below 12 mW per channel with a 1.8 V supply.

As anticipated in Section II, in the first phase, we are pursuing two separate ASIC developments: 1) the analog front-end ASIC, which has been fabricated and characterized as described

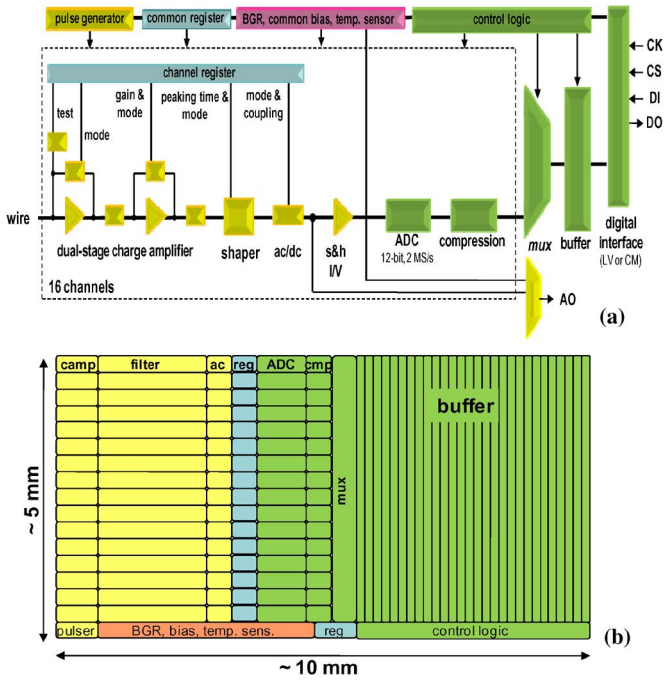

Fig. 11. (a) Block diagram and (b) simplified layout of the proposed front-end mixed-signal ASIC; the projected power dissipation is below 12 mW/channel. The projected size, pads included, is on the order of $6 \times 11\ \mathrm{mm}^2$.

in the next two Sections, and 2) the ADC-buffer ASIC, which is being currently finalized. In designing both ASICs, we applied the guidelines that we expect would provide the required 20-year lifetime.

A. Architecture of the Analog Front-End ASIC

The analog ASIC consists of the front-end section down to the ac/dc coupling stage from Fig. 11(a), including the channel registers and its digital interface. The physical layout is shown in Fig. 12. Access to the individual test structures, used for the characterization reported in Section II, is at the top and bottom of the layout. The input MOSFET is a p-channels biased at 2 mA (3.6 mW) with a L/W ratio of 0.27 μm/10 mm (200 fingers, 50 μm each), in agreement with our conclusions in Section II, followed by a dual cascode stage [34]. At 300 K and 77 K the MOSFET offers, respectively, a $\mathrm{g_m} \sim 45$ mS and ~90 mS and a $\mathrm{C_g} \sim 14$ pF and ~18 pF, operating at IC ~ 0.4 and ~1.25 (i.e., in moderate inversion). The charge amplification is obtained in two stages, each with adaptive reset and nonlinear pole-zero cancellation [35], [36], and it provides a charge gain up to $20 \times 16 = 320$, adjustable to 4.7, 7.8, 14, and 25 mV/fC. The charge amplifier is followed by a high-order semi-Gaussian anti-aliasing filter [37] with adjustable time constant and the ac/dc coupling stage which, when enabled, introduces an ac a time constant on the order of 100 μs. Each channel also implements, not shown in Fig. 11(a), a high-performance analog buffer capable of driving 250 Ω//400 pF and which, in the final version, will be replaced with the sample-and-hold stage preceding the ADC [see Fig. 11(a)]. The buffer will still be used for monitoring the analog signals. In its current version, the

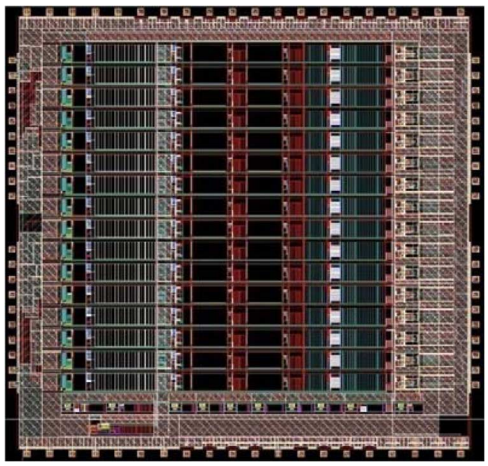

Fig. 12. Physical layout of the analog ASIC, with size $\sim 6 \times 6\ \mathrm{mm}^2$.

analog ASIC is suitable for a possible integration in the MicroBoone LAr TPC detector [38]. The dissipated power is about 5 mW/channel, plus an additional ~5 mW in each output buffer.

The ASIC integrates a band-gap reference (BGR), used to generate all of the internal bias voltages and currents (as ratios between the BGR voltage and a resistor). With a modest dependence of the non-silicided resistors with the temperature (a few percent from 300 K to 77 K, in line with our preliminary results reported in the next section), this bias scheme offers good stability of the operating points over a wide range of temperatures.

In designing the ASIC, the operating points were set to absorb the shifts with the temperature of the MOSFET thresholds (see Fig. 2). The use of voltage feedback configurations with high loop gains and passive feedback components made it possible to contain the dependence on the temperature of the signal response.

B. Preliminary Experimental Results

The ASIC, encapsulated in a standard plastic package, was characterized at room temperature (300 K) and fully submerged in liquid nitrogen (77 K). The text fixture was placed in a dewar and the liquid nitrogen was poured in a few seconds until the fixture was fully submerged. During these tests, the fixture was cycled, without incurring in any issue, more than 50 times between the two environments.

Fig. 13 shows the measured pulse response, along with some details on the adjustment of the gain, peaking time, and baseline. These results are in close agreement with our simulations and indicate that the analog and the digital circuits (including the digital interface) operate as expected in the cryogenic environment. Simulations and experimental results show that the nonlinear pole-zero cancellation at cryogenic temperature needs to be optimized, which will be done in the next revision of the design. The revision will also integrate the test structures for the characterization of the CMOS lifetime and the temperature dependence of the non-silicided resistors.

Charge Sensitivity Calibration: Each channel is equipped with an injection capacitor of nominal value 198 fF (size $10 \times 18\ \mu\mathrm{m}^2$) which can be used for test and calibration and can be

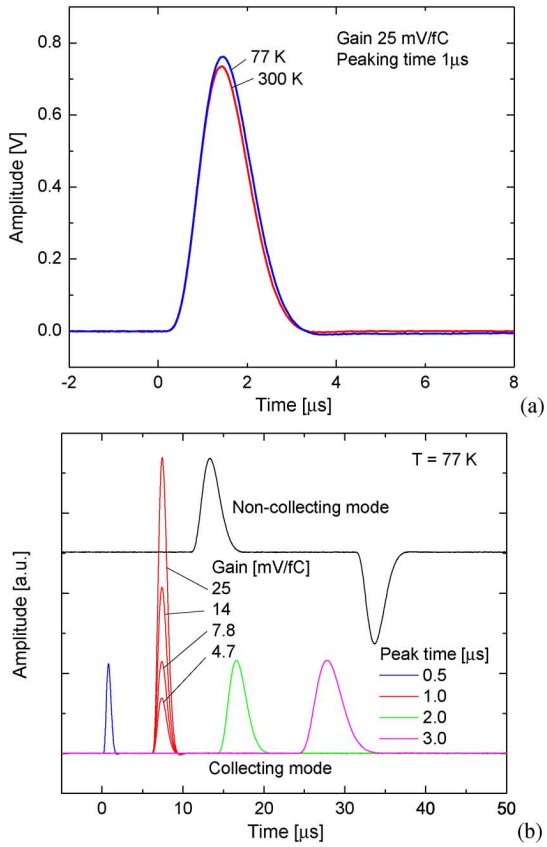

Fig. 13. Measured pulse response at 300 K and 77 K (a), with details (b) on the adjustment of gain, peak time, and baseline.

enabled and disabled through a dedicated internal register. By using a precisely measured external capacitor, we extracted the value of the injection capacitance, equal to 184 fF at 300 K and 183 fF at 77 K, with a change of less than 0.5%. This remarkable result, along with the small change in peaking time with the temperature [Fig. 13(a)], demonstrates a high stability of the passive components (resistors and capacitors). In reference to the band-gap reference circuit, we measured 1.185 V at 300 K and 1.164 V at 77 K, with a decrease of about 1.8 %. The temperature sensor gave 867 mV at 300 K and 259.3 mV at 77 K, with a response of 2.86 mV/K, in close agreement with the simulations as well.

Fig. 14 shows the measured ENC versus the time constant (peaking time) of the entire analog chain (preamplifier, filter, buffer). At 1 μs, we measured $\sim 650\ \mathrm{e}^-$, to be compared to the simulated $\sim 530\ \mathrm{e}^-$ in Fig. 10. If we include in the simulation the contributions from the next stages in the analog chain, we obtain $\sim 600\ \mathrm{e}^-$. The residual difference is due to the thermal noise from the $\sim$ 12 Ω (3 Ω at 77 K) parasitic resistance of the ASIC input lines, which contributes to about 150 e^-. The width of those lines will be increased in the revision in order to reduce it to negligible. A second contribution, on the order of 60 e^-, is due to the dielectric loss from the input capacitor used to simulate the wire, which can be approximated with [39]

$$\mathrm{ENC}_{\mathrm{diel}} \approx \sqrt{2\mathrm{kTC}_{\mathrm{diel}} \cdot \mathrm{tg}(\delta)} \tag{7}$$

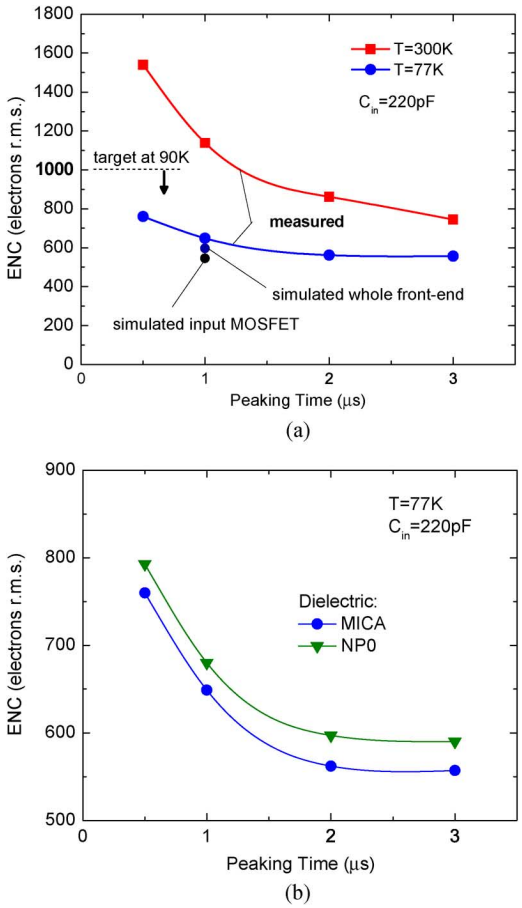

Fig. 14. (a) Measured ENC for the analog ASIC at 300 K and 77 K at the four peaking times. The simulated ENC from the input MOSFET and from the whole analog chain is also shown. (b) Measured ENC using a MICA and a ceramic NPO capacitor to emulate the sense wire capacitance.

where $\mathrm{tg}(\delta)$ is the dielectric loss factor. In Fig. 14(b), we compare the measurements by using MICA and NPO ceramic capacitors, exhibiting dielectric loss at 77 K $\sim 0.1 \times 10^{-3}$ and 2.5×10^{-3}, respectively. It is worth noting that the dielectric loss contribution will not be present with the wire.

C. Architecture of the ADC

The shaped signal which results from the induction in the TPC wires must be sampled and digitized in 12-bit words at a rate of 2 MSamples/s. This is achieved by integrating one ADC in each channel. The ADC, currently being finalized as a separate ASIC, aims at offering the 12-bit resolution, converting in less than 500 ns, and dissipating about 2 mA (3.6 mW). In our design, the power can be reduced at the expense of the conversion time, which scales approximately with the inverse of the current.

The conversion occurs in two stages, the first requiring about 150 ns and providing the six most significant bits (MSBs); and the second requiring about 250 ns and providing the six least-significant bits (LSBs), for a total of 12 bits resolution in about 400 ns. The residual 100 ns are available for encoding and reset.

Both stages (LSB and MSB) are based on the current mode ADC concept described in [34] where the input voltage is sampled, converted into a current, and compared with a number of

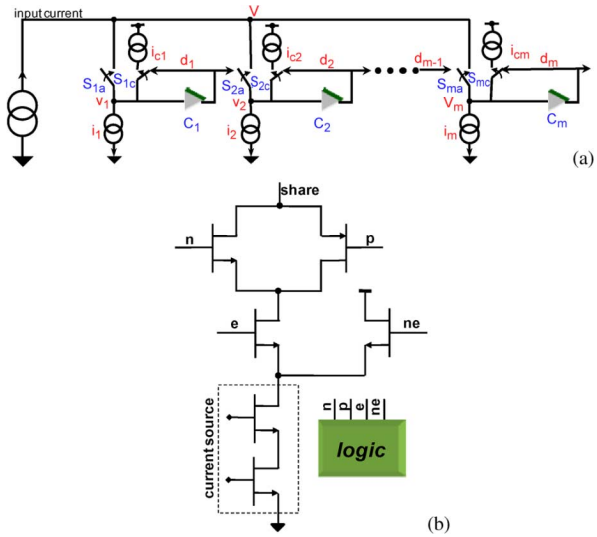

Fig. 15. Simplified schematic of the (a) ADC architecture and (b) individual ADC cell.

matched current cells sequentially enabled. Fig. 15(a) shows a simplified schematic of the ADC structure. The individual cell is shown in Fig. 15(b) and it is composed of a cascoded current source, two MOSFETs controlled by signals e and ne, and providing current steering with positive feedback, two other MOSFETs controlled by signals n and p and working as switches, and a control logic. The layout size is about $1.2\ \mathrm{mm} \times 230\ \mu\mathrm{m}$. Details on the design and layout, along with the experimental results, will be published later.

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