PHX: Tower Section

Ray Yarema, FNAL, June 9th

- Ideal
- Dual Tower
- Outer Segment with Chips and Kapton
- Side View with Chips, Bumps and Kapton
- Inner Segment with Chips and Kapton

Carbon Fiber Support and Cooling
Endcap Readout: Front End

- 6 x 512 channels
- 5 x 512 channels
- Fiber 2.5 Gbit/s
- Slow Control ~100 Hz
- RISC onboard
- OASE chip
- LVDS 6 x 160 MBit
- PHX/FPIX2 is zero suppressed !!!

Hit: 9 bit address, 3 bit adc, 4 bit chip-id, tag 8 bit, i.e. 24 bits

1 % Occupancy translates into:
60 x 24-bits in <0.6 micro seconds!

5 x 512 channels
LINUX PCs in 3d net topology

Endcap Readout: Back End

24 cards each end!

GLink

Fiber 2.5 Gbit/s

OASE chip

PHENIX emulator FPGA

Event Tag

DATA (copy)

Readout Unit (PCI bus)

FPGA

TRACKING FPGA

Level I or II output

4 X (4 wedges)

DATA IN

Arcnet

Slow Control ~100 Hz

PHENIX emulator FPGA