

Current AMU-ADC Testing Results

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INTRODUCTION. This document summarizes the testing results of the PHENIX AMU-ADC chip development as it pertains specifically to MVD requirements. This current chip is the second version to be fabricated using the Hewlett-Packard 1.2 micron CMOS process available through MOSIS. The first design was found to have a short between ground and power due to an unintended contact between diffusion wells. This second version corrected the layout error and also made some other minor changes. Testing on the new chips revealed another layout error where a buffer circuit involved with the serial data string had not been connected to the power bus. This error was easily corrected by Advanced Materials Engineering Research (AMER), otherwise known as the "Silicon Surgeon", by depositing a thin film metal trace to make the connection. After fixing a total of 10 chips, all parts of the new chip now function. The corrected layout change is sufficiently minor to **not** require another prototype fabrication run.

YIELD. MOSIS supplies 25 chips when using the HP CMOS process. Even with the dead serial string, it was possible to do some limited testing by supplying the ADC clock and watching for a Full Scale Count (FSC) to come out after the ADC counter had finished counting 12 bits, or 4096, clock transitions. Using this criteria, all 25 chips appear to be functional. One chip package had a broken pin, so the yield at this point is 24 of 25, with the single reject due to packaging and not to the silicon.

After the 10 chips returned from the Silicon Surgeon, an analog voltage was supplied to all inputs and conversions made on each channel. Again, each chip is completely functional by this criteria.

BASIC PERFORMANCE. A detailed block diagram is shown in Figure 1. The AMU-ADC consists of 32 channels of analog memory (AMU) and each channel consisting of 64 cells of memory addresses. Each AMU channel has a corresponding channel of ADC. The ADC is a Wilkerson type due to the ease of multiple channel applications with very little logic overhead per channel. The counter used is a Gray-code counter and counts both positive and negative clock edges. Double-edged counting places requirements of 50% duty cycle on the fast ADC clock. The counter can be programmed to operate in 9, 10, 11, or 12 bit modes, thus allowing the user to optimize the conversion time with the number of required bits.

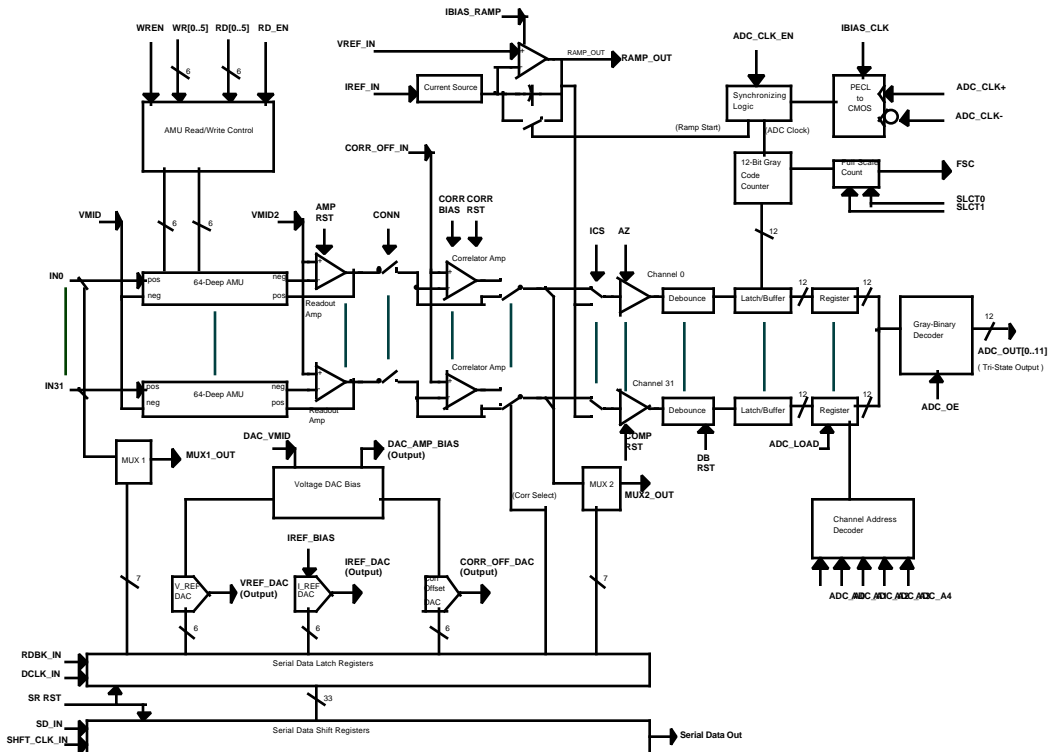


Figure 1. AMUADC detailed block diagram.

The Digital to Analog Converters (DACs) allows for on-chip references for the AMUADC. The ADC uses two references to setup the analog input range. V_{ref} DAC controls the maximum voltage of the ramp generator thus setting the full scale voltage. The I_{ref} DAC controls the slew rate of the ramp signal, and should be adjusted relative to the FSC signal to set the minimum range. The Correlator Offset DAC sets the needed offset voltage for the correlator circuit to use.

POWER REQUIREMENTS. The measured power consumption with the fast ADC clock running at 40 MHz was 9.1 mA at a supply voltage of 5 V. The total current consists of 8.2 mA in the analog section and 0.9 mA for the digital. This gives an average power consumption of $(5\text{ V})(9.1\text{ mA}) = 45.5\text{ mW}$. There is a peak transient current surge during the ADC autozero with a peak value of 23.5 mA. This transient surge lasts for the duration of the autozero, which is 1.4 μs in our test setup. The sample rate is 6.5 ms.

DAC PERFORMANCE. There are three 6-bit DACs on the chip. Two are voltage output used for setting reference voltages as described above, and the third is a current output used for controlling the slew rate of the Ramp Generator. The output voltage range for the V_{ref} DAC is about 0.3V to 4.8V. This allows a wide adjustment range that is adjustable in approximately 75 mV steps. Figures 2-4 below show measured DAC behavior.

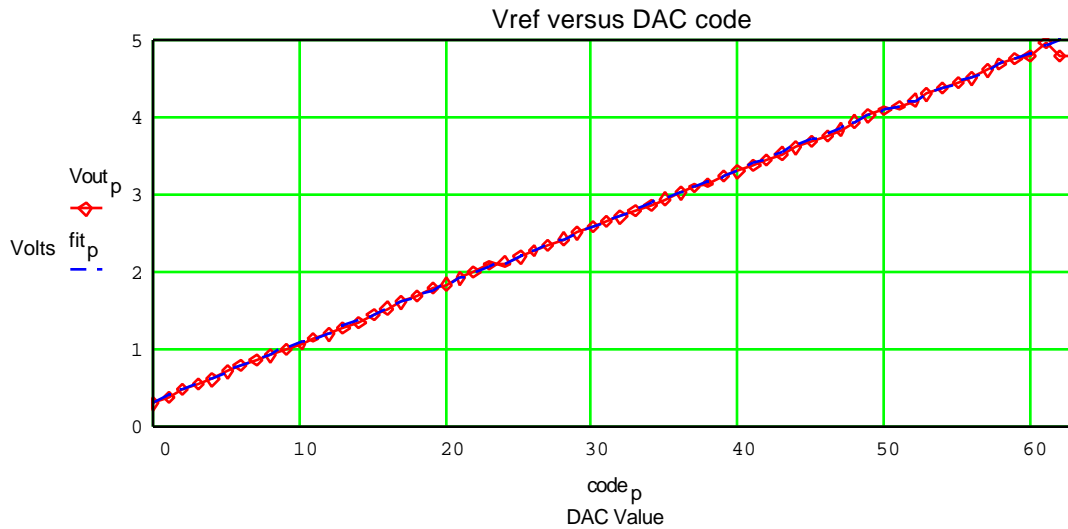


Figure 2. V_{ref} versus Code

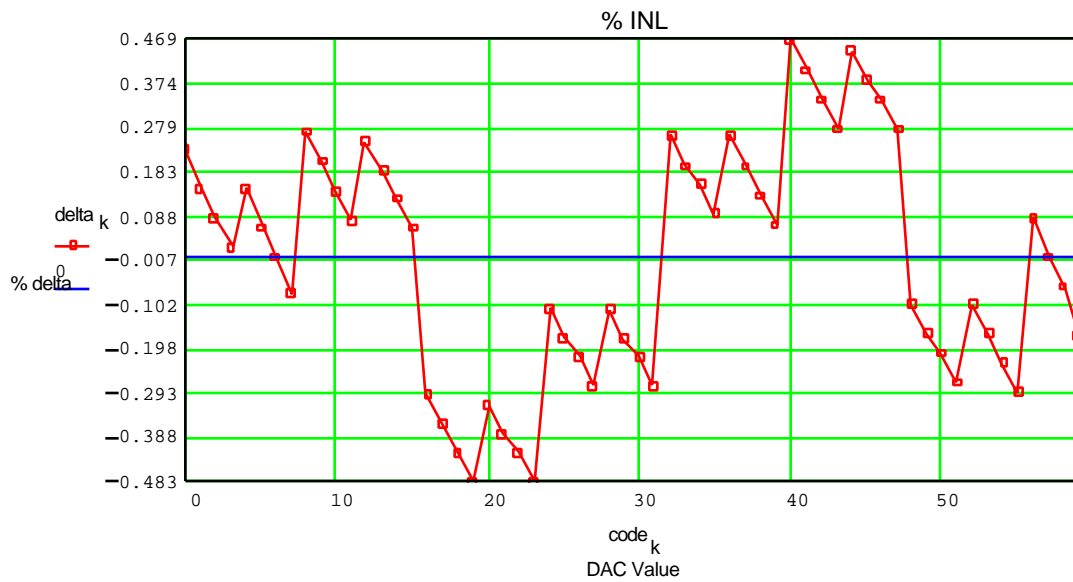


Figure 3. V_{ref} DAC Integral Nonlinearity

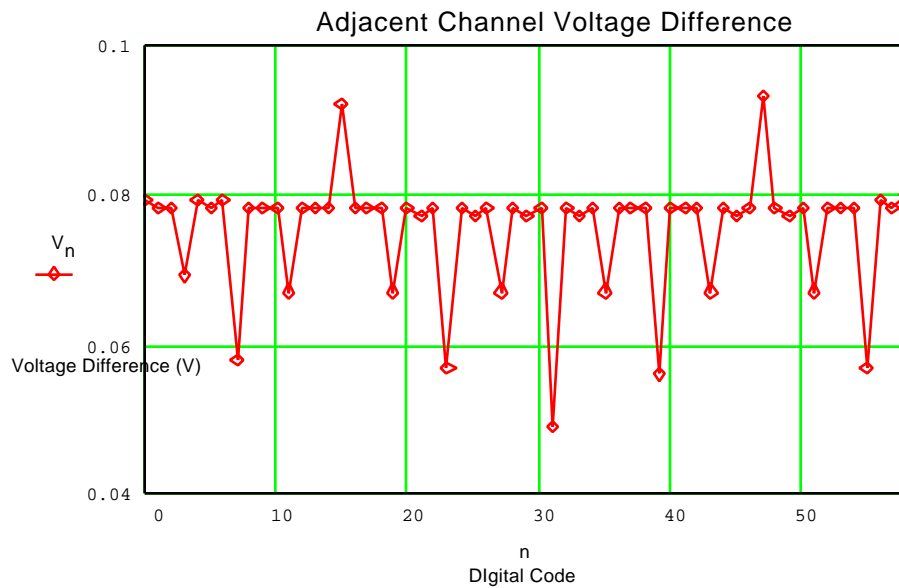


Figure 4. V_{ref} DAC ΔV

The Correlator Offset DAC has an output voltage range of about 0.13 V to 2.4 V. Typical operation of the correlator function would use an offset voltage of about 1.6 V, so this provides a reasonable range of adjustment. Figures 5-8 show measured Correlator Offset DAC behavior.

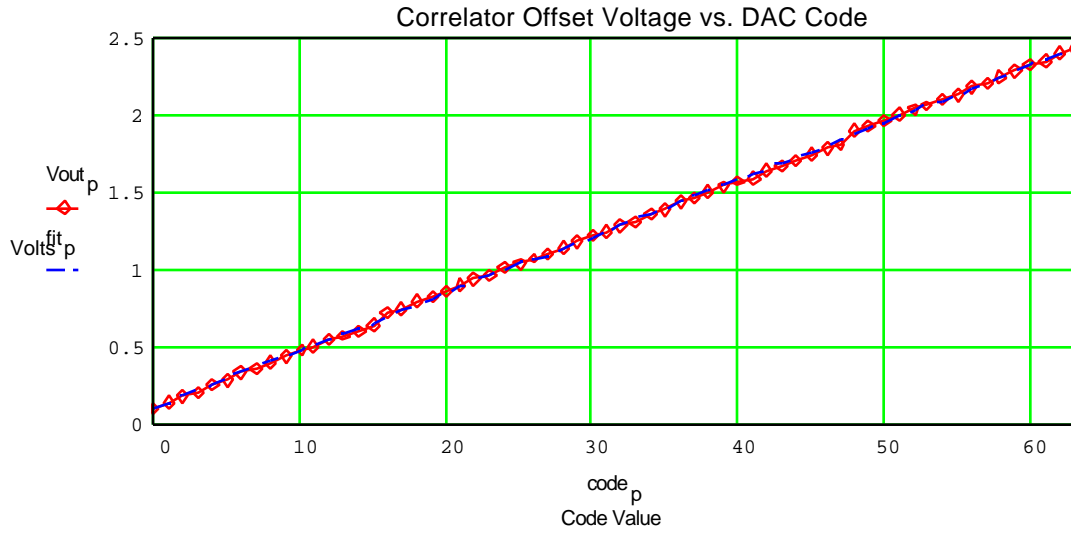


Figure 5. Correlator Offset DAC

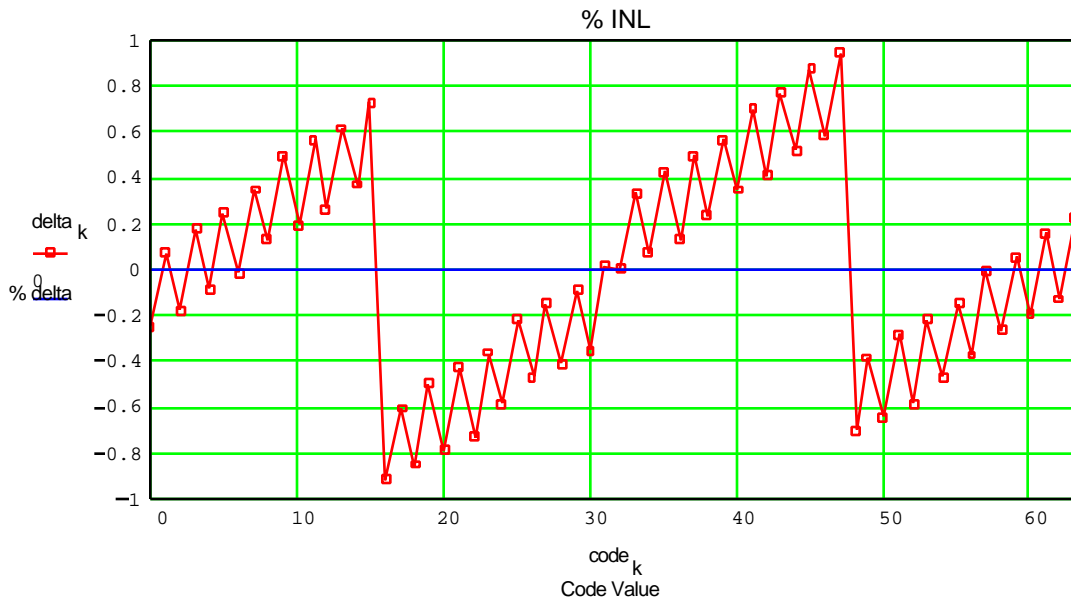


Figure 6. Correlator Offset DAC INL

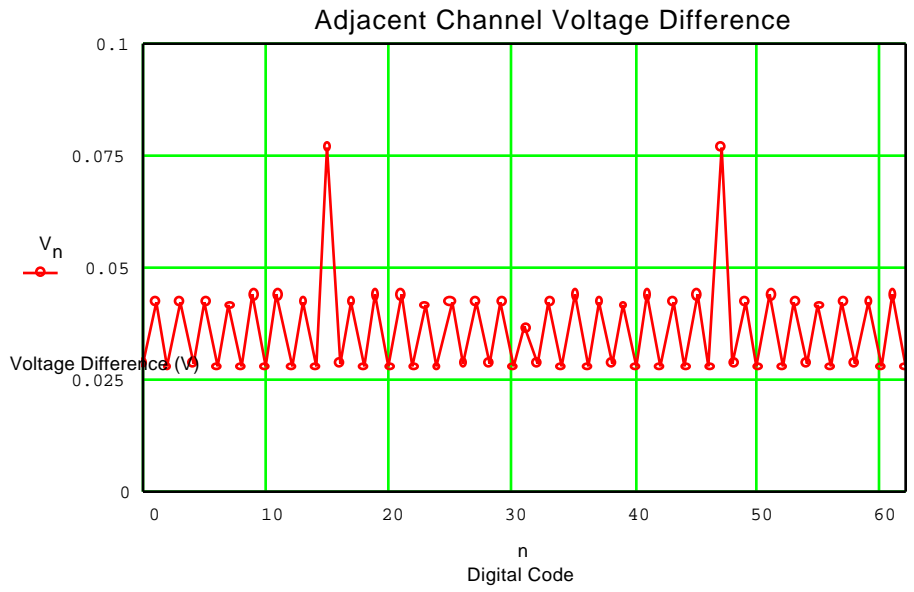


Figure 7. Correlator Offset Voltage DNL

The I_{ref} DAC measured performance is shown below in Figures 8-10. It has an adjustment range of about $1 \mu\text{A}$ to $72 \mu\text{A}$. This wide range is needed to allow adjustment of the ramp slew rate in applications using 12-bit precision at slow ADC clock rates or 9-bit precision at high clock rates.

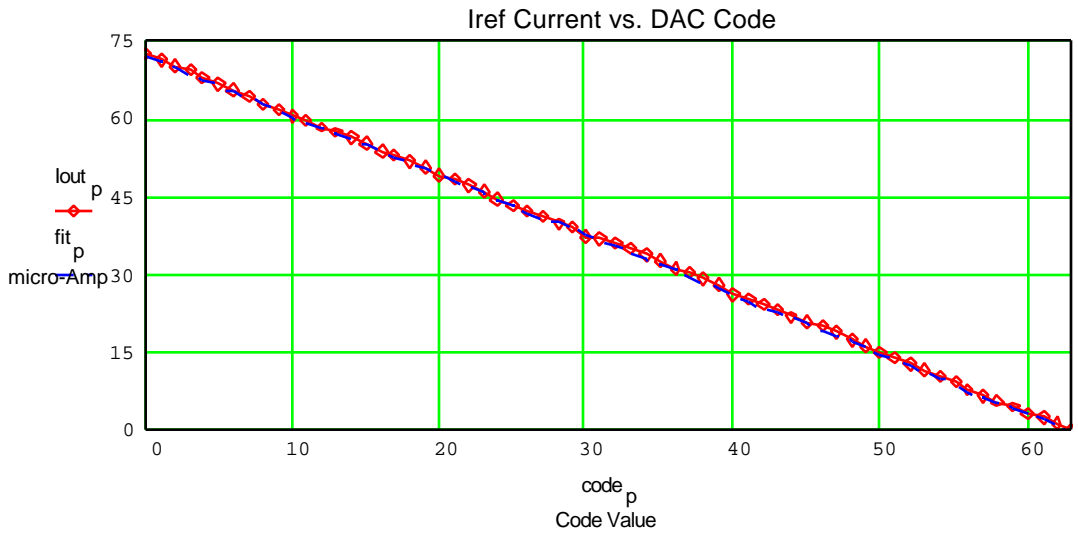


Figure 8. I_{ref} versus Code

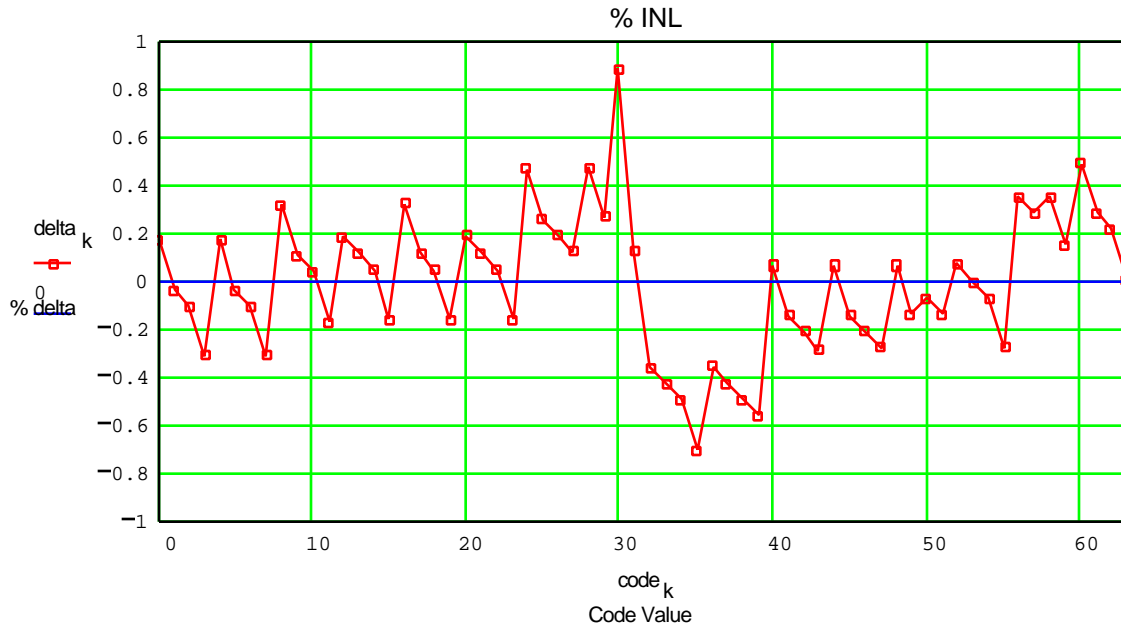


Figure 9. I_{ref} DAC INL

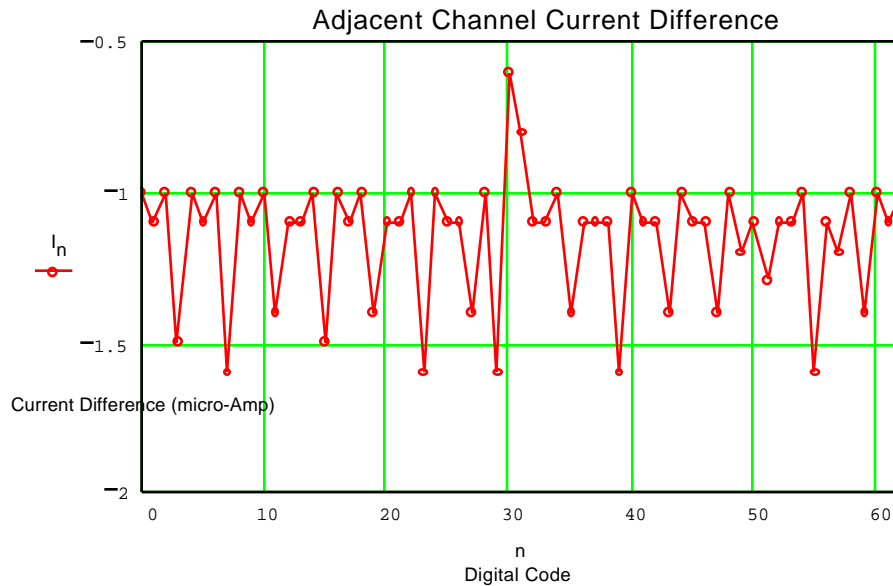


Figure 10. I_{ref} DAC DNL

INTEGRAL NONLINEARITY. Measured INL for the AMUADC chip, using the correlator, is about $\pm 0.2\%$. This is measured with the ADC clock running at 40 MHz and 10-bit mode using single-shot data. Another important figure of merit is the spread of the converted data running multiple samples at the same voltage. Under these conditions, the standard deviation of 1000 samples per voltage was about 0.6 LSB. This is equivalent to Full Width Half Max of 1.4 LSB. Figure 11 shows the measured standard deviation versus ADC output code.

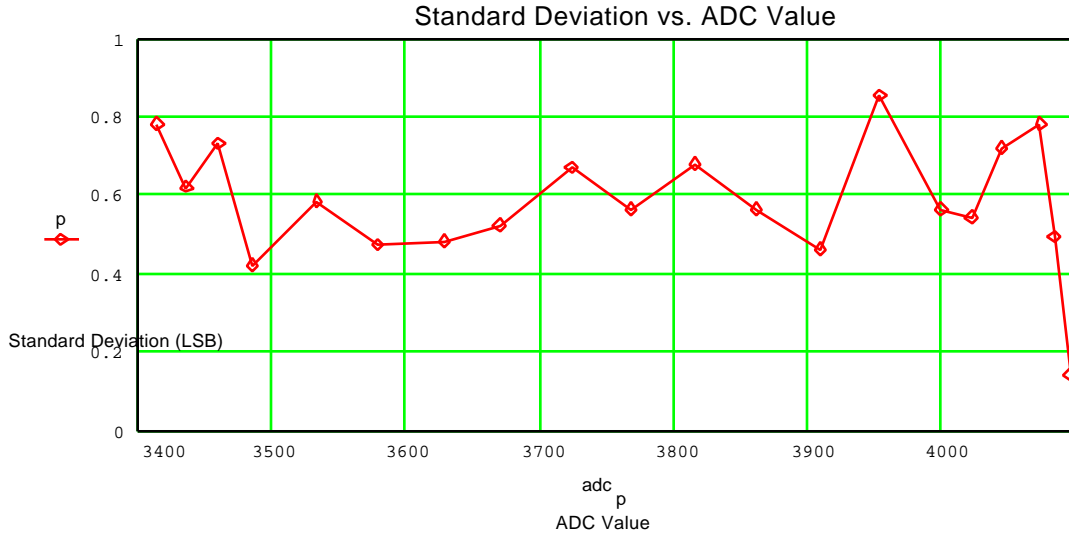


Figure 11. Standard deviation of 1000 samples per point, $F_{ADC} = 40$ MHz, 10 bit mode, and Correlator on.

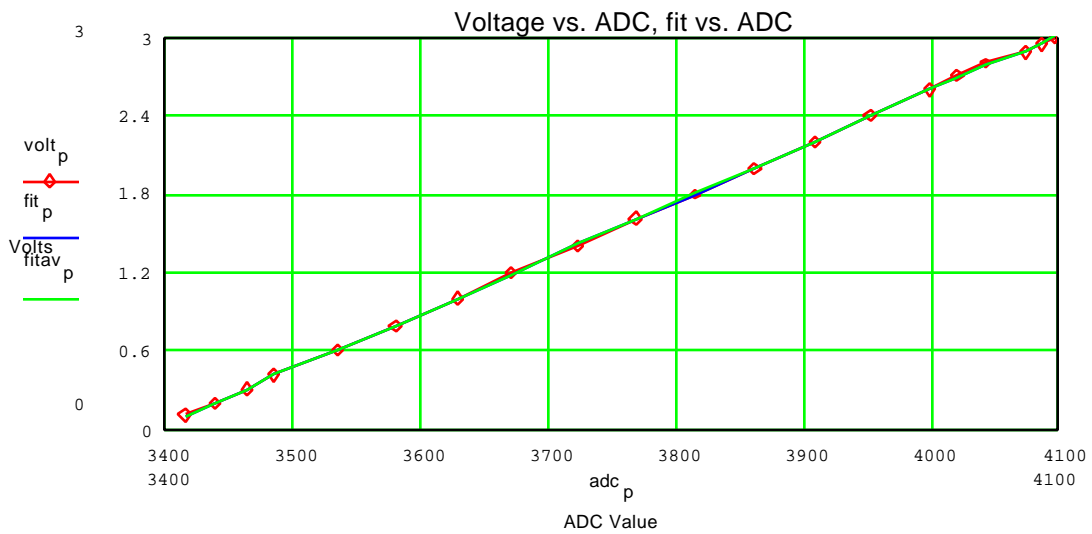


Figure 12. Input voltage, best fit with single-shot data, and best fit with 1000-point averaged data versus output ADC code. Conditions are Correlator = ON, $F_{ADC} = 40$ MHz, and 10-bit mode.

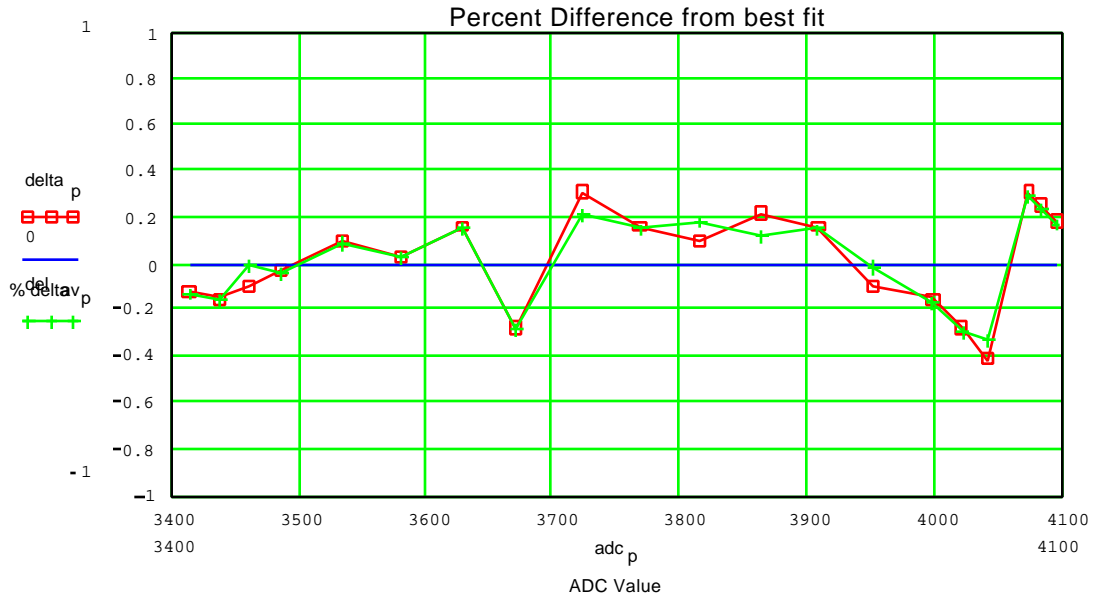


Figure 13. INL of single-shot data and 1000 samples of averaged data. Conditions are Correlator = ON, $F_{ADC} = 40$ MHz, and 10-bit mode.

DIFFERENTIAL NONLINEARITY. DNL measurements using the correlator circuit are extremely difficult to perform with equipment at hand. Therefore the DNL measurements are made without the correlator circuit by applying to the inputs an extremely low frequency triangle wave with a peak to peak amplitude that just exceeds the maximum and minimum conversion range of the ADC. The measured DNL was 87%, and the plotted data is shown in Figure 14.

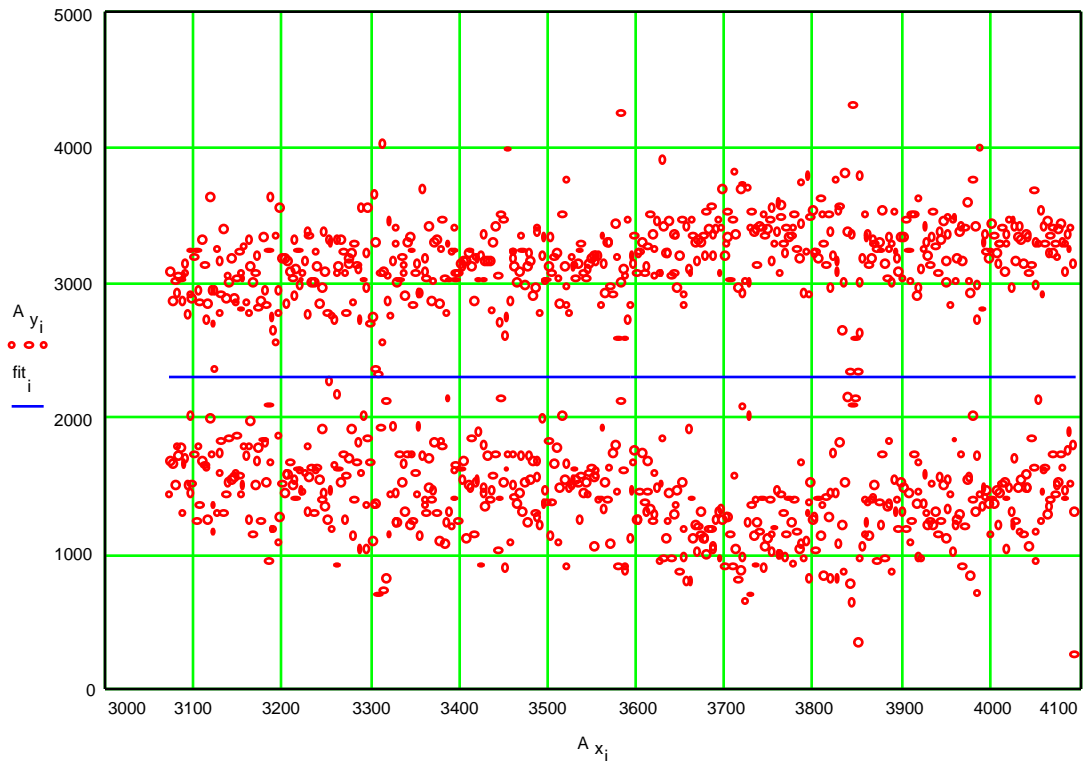


Figure 14. DNL of AMUADC in 10 bit mode.

Figure 14 shows there are no missing codes. However, the data plotted in Figure 14 also reveals some preference for even (decimal) ADC output codes over odd output codes. It is unclear what causes this, but possibilities include a problem with the duty cycle of the ADC clock or with correlated clocking noise somehow contaminating the ADC ramp or comparator circuits. The duty cycle of the clock generator is 50%, so the problem is likely elsewhere. It may be possible to tune out this effect by duty cycle adjustments if the problem is severe enough.

CELL-TO-CELL MATCHING. The software implementation has so far prevented us from performing

Table 1. AMU Pipe Statistics

Pipe:	Mean	Sigma	Pipe:	Mean	Sigma
Pipe 0 =	759	35.5	Pipe 16 =	762	9.9
Pipe 1 =	760	38.6	Pipe 17 =	766	3.8
Pipe 2 =	765	38.3	Pipe 18 =	775	32.9
Pipe 3 =	767	6.7	Pipe 19 =	767	29.9
Pipe 4 =	763	16.5	Pipe 20 =	764	23.9
Pipe 5 =	764	27.6	Pipe 21 =	763	22.0
Pipe 6 =	763	22.9	Pipe 22 =	765	23.8
Pipe 7 =	761	29.0	Pipe 23 =	764	24.1
Pipe 8 =	766	18.9	Pipe 24 =	766	31.5
Pipe 9 =	763	15.5	Pipe 25 =	770	31.8
Pipe 10 =	766	33.0	Pipe 26 =	769	14.7
Pipe 11 =	766	26.6	Pipe 27 =	772	39.1
Pipe 12 =	765	38.5	Pipe 28 =	767	4.4
Pipe 13 =	765	14.3	Pipe 29 =	765	32.9
Pipe 14 =	766	22.5	Pipe 30 =	765	35.5
Pipe 15 =	763	32.2	Pipe 31 =	764	23.8

a cell by cell evaluation over the entire AMU portion of the chip at one time. We can report matching statistics, however. Table 1 shows the mean and standard deviation from sampling each cell 1000 times in each channel with the same analog voltage input.

CHIP TO CHIP MATCHING. Table 2 below shows the measured chip to chip matching of the voltage references, current references, slew rate of the ramp, and the maximum ADC clocking rate. The chip to chip capacitor matching can be indicated by knowing the magnitude of the current reference and the ramp slew rate. I_{ref} is mirrored with a gain of 0.5 to drive an integrating capacitor. The capacitor's design value is 14.8 pF.

Table 2. Chip to Chip Matching data.

Chip #	V_{REF} (Volt)	V_{COR} (Volt)	I_{REF} (μA)	Ramp (V/ μs)	Cap (pF)	Max Freq (MHz)	I_{REF} Mid (μA)
1	4.546	1.588	3.2	0.132	12.12	235	37.2
2	4.539	1.586	3.1	0.170	9.12	230	36.9
3	4.483	1.546	3.2	0.150	10.67	232.5	37.3
4	4.583	1.528	3.1	0.140	11.07	237.5	36.1
5	4.624	1.557	3.2	0.152	10.53	215	36.8
7	4.492	1.559	3.1	0.126	12.30	232.5	36.7
8	4.561	1.535	3.2	0.136	11.77	237.5	37.3
9	4.540	1.525	3.1	0.152	10.20	230	36.4
10	4.387	1.543	3.2	0.112	14.28	230	36.4
11	4.509	1.563	3.1	0.150	10.34	220	36.1

The I_{REF} used when measuring the ramp slew rate was near the lower range of the test setup measuring capability, and therefore the value of the capacitance may not be accurate. The test should be repeated with a larger current that is more easily measured.

CONVERSION TIME. The time needed to execute a conversion is given by Equation 1,

$$t_{conv} = \frac{2^{n-1}}{f} + T_{oh} \quad (\text{Eq. 1})$$

where n is the number of converted bits, f is the ADC clock frequency, and T_{oh} is time needed for setup overhead. The exponent is $(n-1)$, instead of n , because the counter circuit uses both rising and falling clock edges and therefore effectively counts at twice the supplied frequency. This imposes a requirement for a 50% duty cycle clock to ensure equal bin width and good differential nonlinearity (DNL). The overhead time needed when using the correlator circuit in our test setup is 25 μs , so total conversion time in 10-bit mode and running the ADC clock at 40 MHz is 37.8 μs . A minimum of $T_{oh} = 10 \mu\text{s}$ is required for proper operation. See Emery, et al, "Timing and Control Requirements for a 32-Channel AMU-ADC ASIC for the PHENIX Detector" from the Proceedings of the 1997 IEEE Nuclear Science Symposium.

SUMMARY. The AMUADC chip seems to be suitable for use in the MVD subsystem. Used in the multi-chip module the chip will likely work better than in our test stand due to fewer connection parasitics. INL and DNL results are sufficiently low for use in a 10-bit system required by MVD. The Full Width Half Max is sufficiently small to achieve good single-shot performance with real data. Again, the data presented here is focused specifically toward MVD application. Some data is general in nature, but most applies only at modest ADC clock frequencies and using the correlator circuit.

Production AMU_ADC version 2 Pin Definitions

Michael S. Emery
10/24/97 updated 10/24/97

This table describes pin functions for the production version 32-channel AMU_ADC chip.

Package Pin No.	IC Pad No.	Name	Description
1		NC	No Connection
2	82	AGND	Analog Ground. SW Corner.
3	83	MUX1_OUT	Output for monitoring AMU at input. Requires channel address from serial data string.
4	84	CORR_OFF_DAC	DAC output to supply CORR_OFF_IN.
5	85	CORR_OFF_IN	Correlator Offset Input.
6	86	MUX2_OUT	Output for monitoring AMU at output. Requires channel address from serial data string.
7	87	IREF_DAC	DAC current output to supply IREF_IN.
8	88	IREF_IN	Sets slew rate for ADC Ramp Generator.
9	89	IBIAS_RAMP	Bias current for Ramp Generator circuit. Internal biasing provided, but may be modified externally with resistor network.
10	90	VREF_DAC	DAC output to supply VREF_IN.
11	91	VREF_IN	Reference Voltage for ADC. Sets the starting voltage of the ADC Ramp. Vref 4.8V
12	92	AVDD7	Analog VDD. Typical Vdd = 5V.
13	93	AGND7	Analog Ground.
14	94	DAC_AMP_BIAS	Bias monitor pin for DAC bias. (Output, hi Z)
15	95	DAC_VMID	Input reference voltage. Typical = Vdd / 2
16	96	NC	Ground to most convenient ground.
17	97	IREF_BIAS	Bias for DAC used for IREF. Internal biasing provided, but may be modified externally with resistor network.
18	98	AGND4	Analog Ground. Comparator. Same as i.c. pad number 23. Both connections are needed.
19	99	AVDD4	Analog VDD. Typical Vdd = 5V. Comparator. Same as i.c. pad number 22. Both connections are needed.
20	100	DVDD3	Digital Vdd. Typical Vdd = 5V.
21	101	DGND3	Digital Ground
22	102	SD_IN	Serial Data input
23	103	SR_RST	Serial Data reset input. Active HIGH.
24	104	WREN	AMU Write Enable input. Active HIGH.
25	105	WR0	AMU Write Address 0
26	106	WR1	AMU Write Address 1
27	107	WR2	AMU Write Address 2
28	108	WR3	AMU Write Address 3
29	109	WR4	AMU Write Address 4
30	110	WR5	AMU Write Address 5
31	111	DCLK_IN	Latches serial data. Rising edge. Input.
32	112	RDBK_IN	Readout latched serial data for verification. Input. Logic 1 - Readback; Logic 0 - input. See Serial Data String documentation for proper protocol.
33	113	SHFT_CLK_IN	Shift register clock input for Serial Data input. Typical frequency 1 MHz. Rising Edge. See Serial Data String documentation for proper protocol.
34	114	SD_OUT	Serial Data Out.
35	115	SLCT1	ADC Mode Conversion bit 1. 00 = 9 bit, 01 = 10 bit, 10 = 11 bit, and 11 = 12 bit ADC conversions (SLCT1,SLCT0). Input.
36	116	SLCT0	ADC Mode Conversion bit 0. 00 = 9 bit, 01 = 10 bit, 10 = 11 bit,

			and 11 = 12 bit ADC conversions. Input.
37	117	IBIAS_CLK	Bias for ADC high-speed PECL-CMOS clock circuit. Internal biasing provided suitable for low-speed operation, but may be modified externally with resistor network. For high-speed operation connect resistor (typically 40K) between VDD (digital) and IBIAS_CLK.
38	118	ADC_CLK_EN	ADC Clock Enable input. Assert high. Starts a conversion by starting the Ramp Generator and Counter simultaneously. Remains high until FSC. (ADC_CLK_EN resets adc counter when low.)
39	119	DVDD	Digital VDD. Typical Vdd = 5V. SE Corner.
40		NC	No Connection
41		NC	No Connection
42		NC	No Connection
43		NC	No Connection
44		NC	No Connection
45		NC	No Connection
46		NC	No Connection
47		NC	No Connection
48		NC	No Connection
49		NC	No Connection
50	120	ADC_CLK+	High speed clock input for ADC. Requires 50% duty cycle, PECL logic levels. Maximum frequency 210 MHz. Complement of ADC_CLK-.
51	121	ADC_CLK-	High speed clock input for ADC. Requires 50% duty cycle, PECL logic levels. Maximum frequency 210 MHz. Complement of ADC_CLK+.
52	122	FSC	Full Scale Count. This output indicates (active High) that an ADC conversion is complete. Data is now ready for loading and read out.
53	123	ADC_A4	ADC channel address 4.
54	124	ADC_A3	ADC channel address 3.
55	125	ADC_A2	ADC channel address 2.
56	126	ADC_A1	ADC channel address 1.
57	127	ADC_A0	ADC channel address 0.
58	128	ADC_OE	ADC Output Enable. Output is High Z when ADC_OE is low.
59	129	DGND2	Digital Ground.
60	130	DVDD2	Digital Vdd. Typical Vdd = 5V.
61	131	ADC_OUT0	ADC Output bit 0. (LSB)
62	1	ADC_OUT1	ADC Output bit 1.
63	2	ADC_OUT2	ADC Output bit 2.
64	3	ADC_OUT3	ADC Output bit 3.
65	4	ADC_OUT4	ADC Output bit 4.
66	5	ADC_OUT5	ADC Output bit 5.
67	6	ADC_OUT6	ADC Output bit 6.
68	7	ADC_OUT7	ADC Output bit 7.
69	8	ADC_OUT8	ADC Output bit 8.
70	9	ADC_OUT9	ADC Output bit 9.
71	10	ADC_OUT10	ADC Output bit 10.
72	11	ADC_OUT11	ADC Output bit 11. (MSB)
73		NC	No Connection
74		NC	No Connection
75		NC	No Connection
76		NC	No Connection
77		NC	No Connection
78		NC	No Connection
79		NC	No Connection
80		NC	No Connection

81		NC	No Connection
82		NC	No Connection
83		NC	No Connection
84		NC	No Connection
85	12	DGND	Digital Ground. NE Corner.
86	13	DGND1	Digital Ground
87	14	DVDD1	Digital Vdd. Typical Vdd = 5V.
88	15	ADC_LOAD	Input. Load ADC Data into latch. Assert high.
89	16	DB_RST	Input. ADC Debounce Reset. Reset debounce circuits. Assert high.
90	17	COMP_RST	Input. ADC Comparator Reset. Assert high.
91	18	AZ	Input. ADC Auto-Zero. Assert high.
92	19	ICS	Input. ADC Internal Comparator Switch. ICS=0 looks at analog input signal; ICS=1 looks at RAMP.
93	20	FRAMEBREAK	Ground to most convenient ground.
94	21	RAMP_OUT	ADC RAMP output signal. Starts high (at VREF) and slews negative toward 0V.
95	22	AVDD3	Analog Vdd. Typical Vdd = 5V. Comparator. Same as i.c. pad number 99. Both connections are needed.
96	23	AGND3	Analog Ground. Comparator. Same as i.c. pad number 98. Both connections are needed.
97	24	AGND6	Analog Ground.
98	25	AVDD6	Analog Vdd. Typical Vdd = 5V.
99	26	VMID2	Input reference voltage. Typical = Vdd / 2
100	27	FRAMEBREAK	Ground to most convenient ground.
101	28	CORR_BIAS	Bias current for Correlator circuit. Internal biasing provided, but may be modified externally with resistor network.
102	29	CORR_RST	Correlator Reset input for AMU Correlator circuit. Assert high.
103	30	AMP_RST	Reset input for AMU readout buffer amplifier. Assert high.
104	31	CONN	Connects AMU output to ADC (or Correlator). Input. Assert high.
105	32	RD5	AMU Read Address 5.
106	33	RD4	AMU Read Address 4.
107	34	RD3	AMU Read Address 3.
108	35	RD2	AMU Read Address 2.
109	36	RD1	AMU Read Address 1.
110	37	RD0	AMU Read Address 0.
111	38	RD_EN	Read Enable input for AMU. Assert high.
112	39	DGND4	Digital Ground.
113	40	DVDD4	Digital Vdd. Typical Vdd = 5V.
114	41	FRAMEBREAK	Ground to most convenient ground.
115	42	AGND2	Analog Ground.
116	43	AVDD2	Analog Vdd. Typical Vdd = 5V.
117	44	VMID	Input reference voltage. Typical = Vdd / 2
118	45	AVDD	Analog Vdd. Typical Vdd = 5V. NW Corner
119		NC	No Connection
120		NC	No Connection
121		NC	No Connection
122		NC	No Connection
123	46	AVDD1	Analog Vdd. Typical Vdd = 5V.
124	47	AGND1	Analog Ground.
125	48	IN0	Input channel 0
126	49	IN1	Input channel 1
127	50	IN2	Input channel 2
128	51	IN3	Input channel 3
129	52	IN4	Input channel 4
130	53	IN5	Input channel 5
131	54	IN6	Input channel 6

132	55	IN7	Input channel 7
133	56	IN8	Input channel 8
134	57	IN9	Input channel 9
135	58	IN10	Input channel 10
136	59	IN11	Input channel 11
137	60	IN12	Input channel 12
138	61	IN13	Input channel 13
139	62	IN14	Input channel 14
140	63	IN15	Input channel 15
141	64	IN16	Input channel 16
142	65	IN17	Input channel 17
143	66	IN18	Input channel 18
144	67	IN19	Input channel 19
145	68	IN20	Input channel 20
146	69	IN21	Input channel 21
147	70	IN22	Input channel 22
148	71	IN23	Input channel 23
149	72	IN24	Input channel 24
150	73	IN25	Input channel 25
151	74	IN26	Input channel 26
152	75	IN27	Input channel 27
153	76	IN28	Input channel 28
154	77	IN29	Input channel 29
155	78	IN30	Input channel 30
156	79	IN31	Input channel 31
157	80	AGND5	Analog Ground.
158	81	AVDD5	Analog Vdd. Typical Vdd = 5V.
159		NC	No Connection
160		NC	No Connection

Table 3. List of Serial Data String, listed in order of first-in to last-in.

Bit #	Label	Function	Bit #	Label	Function
1	MUX2_OE	Mux 2 Output Enable	18	DAC2_4	DAC Corr Code bit 4
2	MUX2_0	Mux 2 Address LSB	19	DAC2_5	DAC Corr Code bit 5
3	MUX2_1	Mux 2 Address bit 1	20	DAC1_0	DAC Iref Code bit 0
4	MUX2_2	Mux 2 Address bit 2	21	DAC1_1	DAC Iref Code bit 1
5	MUX2_3	Mux 2 Address bit 3	22	DAC1_2	DAC Iref Code bit 2
6	MUX2_4	Mux 2 Address bit 4	23	DAC1_3	DAC Iref Code bit 3
7	CORR_SEL	Correlator Select control bit	24	DAC1_4	DAC Iref Code bit 4
8	DAC3_0	DAC Vref Code bit 0	25	DAC1_5	DAC Iref Code bit 5
9	DAC3_1	DAC Vref Code bit 1	26	MUX2-HIZ	Mux 2 pull-down
10	DAC3_2	DAC Vref Code bit 2	27	MUX1-HIZ	Mux 1 pull-down
11	DAC3_3	DAC Vref Code bit 3	28	MUX1_OE	Mux 1 Output Enable
12	DAC3_4	DAC Vref Code bit 4	29	MUX1_0	Mux 1 Address LSB
13	DAC3_5	DAC Vref Code bit 5	30	MUX1_1	Mux 1 Address bit 1
14	DAC2_0	DAC Corr Code bit 0	31	MUX1_2	Mux 1 Address bit 2
15	DAC2_1	DAC Corr Code bit 1	32	MUX1_3	Mux 1 Address bit 3
16	DAC2_2	DAC Corr Code bit 2	33	MUX1_4	Mux 1 Address bit 4
17	DAC2_3	DAC Corr Code bit 3			