LOW NOISE, LOW POWER DISSIPATION ANALOG LSI ELECTRONICS FOR HEAVY ION DETECTORS[1]

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ABSTRACT

The work performed to date for the Multiplicity-Vertex Detector (MVD) for the PHENIX detector collaboration at the Relativistic Heavy Ion Collider (RHIC) is presented in this paper. Composed of approximately 34,000 channels of both silicon strips and silicon pads, the detector per-channel signal processing chain consists of a preamplifier-gain stage, a current-mode summed multiplicity discriminator, a 64-deep analog memory (simultaneous read-write), an analog correlator and a 10-bit 5 μs ADC. All timing control, data buffering, and data formatting for a single 256-channel multi-chip module (MCM) is performed by the system controller or Heap Manager. Each chip set is partitioned into 32-channel sets. Prototype performance for the various blocks will be presented as well as the ionizing radiation damage performance of the 1.2 μ nwell CMOS process used for fabrication.

1. INTRODUCTION

The requirements of low-power consumption, small physical area, a channel count of approximately 34,000, and flexible data handling make the MVD of the PHENIX detector at RHIC one of the most challenging of the PHENIX detector subsystems. Additional requirements, which include a minimum 20:1 signal-to-noise ratio for a single Minimum Ionizing Particle (MIP) signal (which results in noise less than 2500 electrons rms) and discrimination of a 0.5 MIP event for the per-channel multiplicity discriminator, offer a challenging set of problems.

This paper presents measurements of the prototype circuits including the preamplifier-discriminator, analog memory unit (AMU), analog-digital converter (ADC) and heap manager for the MVD detector front-end electronics (FEE).

2. ELECTRONICS ARCHITECTURE

A block diagram of the electronics is shown in Fig. 1. This includes the preamplifier, discriminator, current-sum output, analog memory-correlator and ADC. The system controller, or Heap Manger, is not shown but will also be discussed.

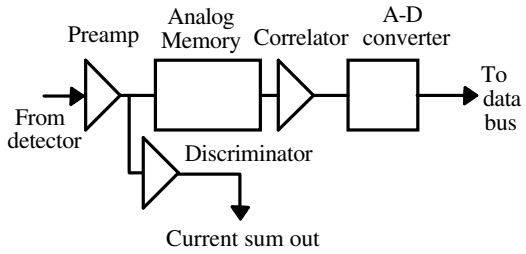

Figure 1. System block diagram.

The electronics will be mounted on a MCM. Each MCM will be connected to 256 detectors and will contain 8 preamplifier-discriminator chips and 8 analog memory-ADC chips. Each of these chips will contain 32 channels of its respective functions. In addition, the MCM will contain the Heap Manager chips and associated control logic. The present prototype chips contain 8 channels of respective functions.

2.1. Preamplifier

The preamplifier utilizes a PMOS cascode amplification stage for low 1/f noise. The input device operates in weak

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inversion with a drain current of 100 μA. Versions of this design are presently being used by not only PHENIX, but PHOBOS detector collaboration [1] (also at RHIC), and the Naval Research Laboratories (NRL) for Germanium spectroscopy [2]. Since the output will be processed by a correlated sampler, the PHENIX and PHOBOS versions employ wideband gain stages after the preamplifier. The NRL version employs a semi-Gaussian shaper with 7 μs peaking time. A summary of the performance of the three versions is presented in Table 1. The resultant power dissipation of the PHENIX preamplifier with the wideband gain stages is approximately 1.2 mW. The circuit is fabricated in 1.2-μ n-well CMOS and has an 85 μ pitch.

Parameter	PHENIX (224 ns double correlated)	PHOBOS (Wideband)	NRL (7 μs peaking)
0 pF noise	660 e	750 e	205 e
Slope	69 e/pF	30 e/pF	8 e/pF
Gain	44 mV/fC	4.2 mV/fC	11 mV/fC
Drain current	100 μA	200 μA	100 μA

Table 1. Performance of various preamplifier versions.

2.2 Discriminator

The multiplicity discriminator block diagram is presented in Fig. 2. Each time an input step greater than the threshold setting is detected, a fixed-value current source is switched to a summing node. The current-mode outputs of 256 discriminators are summed in this manner to produce a multiplicity output whose amplitude is proportional to the number of fired discriminators.

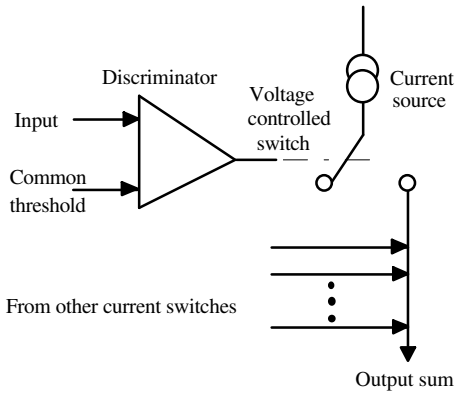

Figure 2. Block diagram of the discriminator.

The design allows triggering at every beam crossing (108 ns) with no deadtime and has a total power consumption of approximately 500 μW/channel.

2.3 Analog memory-correlator

The analog memory unit (AMU) is a 64-cell deep, voltage-write-voltage-read, deadtime-less topology with a power dissipation of approximately 1 mW/channel. The memory is followed by an analog correlator that performs the double-correlated sampling. Both direct memory output and correlated output are available to the subsequent analog-digital converter (ADC). The memory reading and writing is addressed externally from the Heap Manager. The read and write logic decoders are completely independent to allow simultaneous read-write (deadtime-less) operation. A block diagram of the memory is presented in Fig. 3.

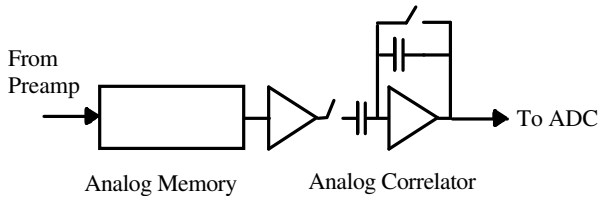

Figure 3. Memory block diagram.

2.4 Analog-digital converter

To allow easy maintainability and take advantage of the economics of scale, the readout architecture of the subsystems within the PHENIX detector have been designed to resemble one another. Using the same parts in many subsystems reduces the needed stocks of spares and simplifies troubleshooting. The economics of scale can be taken advantage of by fabricating a large quantity of one part and using it in many subsystems within the detector. This philosophy is best exhibited in the AMU/ADC chip. A universal AMU/ADC chip that will be used in several subsystems is currently being designed. The architecture of the chip is 32 channels of 64-deep AMU and 32 channels of switchable 10-, 11-, 12-bit ADC. Due to dynamic range requirements, the MVD ADC will be set for 10-bit operation.

The analog-digital converter (ADC), presented in Fig. 4, is a 10-bit Wilkinson type [3] with a maximum dynamic range of 4.5 Volts. The prototype chip implements an eight channel version of the ADC.

The ADC uses 3.75 μW/MHz/channel in the digital circuitry and 6.5 mW total in the ramp generator. This results in a power dissipation of approximately 0.6 mW/channel for a 32-channel chip or 1.19 mW/channel

for the 8-channel prototype at 100 MHz clock frequency (5 μs conversion time for 10-bit conversions).

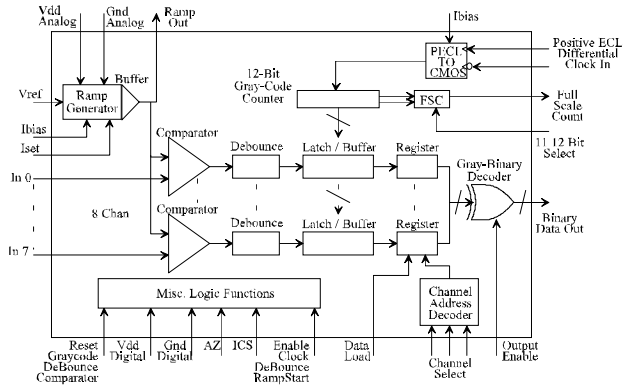

Figure 4. Block diagram of the ADC chip.

2.5 Heap Manager

The Heap Manager controls all on-board functions including AMU address list management and control (for asynchronous read and write operations), correlator timing, Level-1 buffering associated with trigger latency, ADC precharge/acquisition/conversion control, data handling, command interpretation/execution, and timing.

This function has been implemented using commercially available FPGAs allowing in-circuit programmability for future functional upgrades. A multi-function serial interface is used for FPGA programming, calibration setup, diagnostics and monitoring.

A generic Heap Manager has been developed for use in all PHENIX detector subsystems using analog memory for front-end signal buffering during the Level-1 trigger decision; however, due to the reduced size and power requirements for the MVD, this functional block has been partitioned such that the minimum required electronics are physically located near the detectors. The remaining circuitry resides at the ends of the detector subassembly as interface cards to the data collection modules (DCMs). Figure 5 is a block diagram of the MVD Heap Manager showing the basic functional blocks and system partitioning.

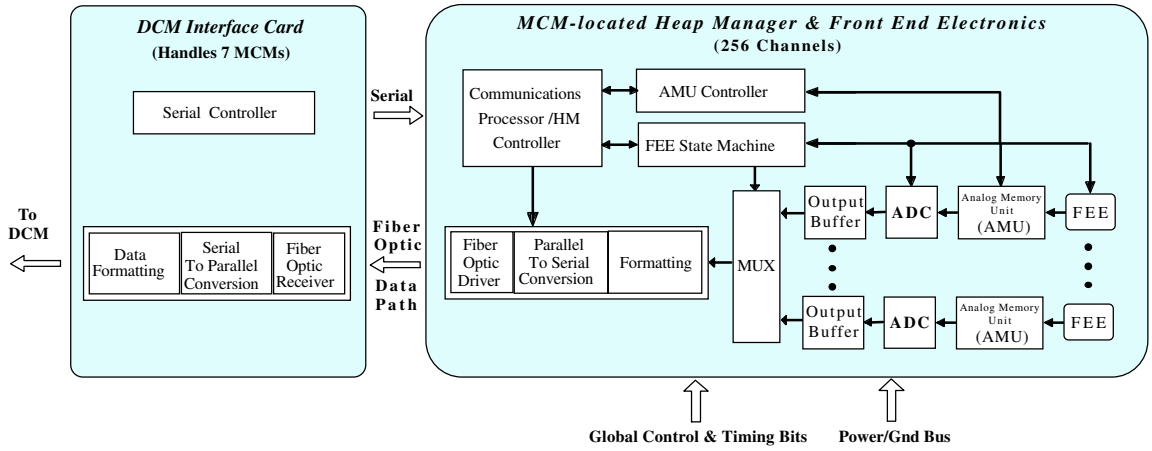

Figure 5. Block diagram of the Heap Manager.

3. RADIATION EFFECTS

Due to the proximity of the detector to the interaction region, some significant (>20 krad) radiation exposure is expected. The desire to utilize a standard non-radiation hardened 1.2 μ CMOS process, resulted in the need for radiation effect measurements to be performed to ensure acceptable circuit operation. Versions of the preamplifier, analog memory and ADC circuits have been irradiated to various doses of ionizing radiation. The process appears to be sufficient for doses to 75 krad for most functions. The major problem lies in the leakage current of the input

protection for the preamplifier. Devices used for protection networks begin to exhibit increased leakage current due to radiation-induced decrease in the nmos threshold voltage. Continuing effort is being made to investigate improved input protection.

4. CONCLUSIONS

The circuits for the PHENIX MVD have been presented. The readout consists of preamplifier, multiplicity discriminator, analog memory, ADC and Heap Manager controller. Prototypes of the major functional blocks have been fabricated and tested. The radiation tolerance of the CMOS process is presently under test.

5. ACKNOWLEDGMENT

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6. REFERENCES

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