1

Charge Sensitive Preamplifier and Pulse Shaper using CMOS process for Germanium Spectroscopy

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Abstract

We have developed a low noise, low power charge sensitive amplifier and pulse shaping circuit. Our application is for a double-sided germanium strip detector, nominally providing 50 independent spectroscopy channels. An array of these detectors would provide significant improvements in imaging, spectroscopy and sensitivity for space-based gamma-ray astronomy. The key features of these electronics are low noise, very low power, and a small footprint per channel. Performance of our first circuit is in good agreement with simulations, with $\sim 205e$ noise rms (0 pF), and 3 mW/channel power consumption. Dynamic range is 0–3.3 MeV (germanium) with a linearity of $\pm 0.6\%$. Performance of this prototype device will be discussed.

I. INTRODUCTION

Gamma-ray astrophysics has made tremendous progress in the last five years following successful missions such as the Soviet *GRANAT* spacecraft and the U.S. *Compton* Gamma Ray Observatory. Future progress in this field will require the development of new detector technologies to improve on each of the key performance characteristics: imaging, spectroscopy, and sensitivity. Our approach to addressing these needs of gamma-ray astrophysics is to develop double-sided germanium strip detectors which combine good energy resolution with fine spatial resolution in a single device. A discussion of single-sided strip detectors is provided by Luke [1] and double-sided detectors by Kroeger [2, 3]. There are several attractive instrument concepts where these detectors may be ideal. The simplest may be at the focal plane of a gamma-ray concentrator such as a super-mirror [4] where a single detector with $\sim$1 mm spatial resolution will provide images and spectroscopy from 5–100 keV with a few arc minute angular resolution. A more ambitious application would configure these detectors in a large array and construct either a coded-aperture imaging telescope, a Compton-scatter telescope, or a combined instrument using both techniques in a single package. Performance of a combined instrument could address the future needs of gamma-ray astronomy over the broad energy range from 20 keV–10 MeV [5].

A single germanium strip detector may have 50 or more strips, depending on the position resolution required by the application. Two-dimensional read-out detectors have strips on both faces of the device, producing signals with opposite polarities. Each strip is independently read out using a low noise spectroscopy amplifier. A large array may ultimately require many thousands of channels of spectroscopy, a configuration with minimum weight and volume, and operation on a tight power budget. An attractive approach to the electronics is through the use of custom CMOS spectroscopy amplifiers, peak-detectors, and ADCs. Similar CMOS devices providing good spectroscopy have been developed for silicon vertex detectors [6, 10], double-sided silicon strip detectors [7], and single-sided silicon strip detectors [8]. However, these electronics are optimized for spectroscopy with silicon detectors. Germanium strip detectors require electronics that are optimized for higher detector capacitance, accept larger signals, yet provide very low noise performance. Peaking times on the order of 8 μs (preamp noise corner of our device) provide the lowest noise for germanium detectors, whereas typical CMOS electronics developed for silicon strip detectors have peaking times less than 200 ns. In our application, detector capacitance is $\sim$10 pF, signals are $\leq 10^6$ electrons, and the electronic equivalent noise charge (ENC) should be ≤ 300 electrons rms. We have developed CMOS amplifiers with low power and low noise appropriate for use with these detectors.

II. FRONT-END ELECTRONICS

The preamplifier design is based on the *"Thin Glenn"* family of preamplifiers developed by Oak Ridge National Laboratory (ORNL) for silicon track detectors in the *PHENIX* and *PHOBOS* projects for the Relativistic Heavy Ion Collider. The heritage of the *Thin Glenn* design came from the

*This work was supported in part by the Office of Naval Research and NASA, under contract No. W–18486.

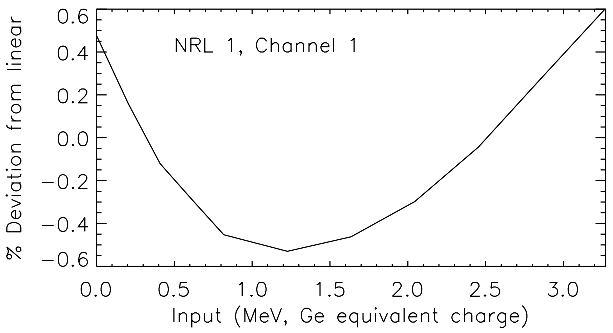

Figure 1: Integral linearity measurment of the CMOS preamplifier and shaping amplifier, *NRL-1*. Plotted are the residuals from a best-fit linear model, relative to the full scale response at 3.3 MeV.

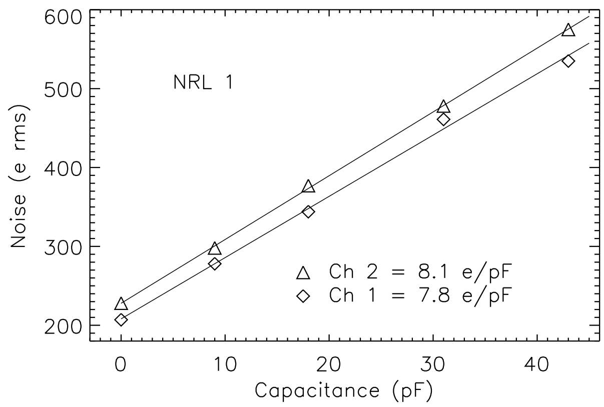

Figure 2: ENC *vs.* detector capacitance for *NRL-1*. The front end p-channel MOSFET for channel 2 has twice the gate area as channel 1. The curves suggest that the smaller gate area provides slightly better performance.

AMPLEX chip developed for CERN [9], followed by the BVX chip [6] developed by ORNL. The fabrication is done with the Orbit 1.2μm CMOS process, and operates from a single 5 V supply. The preamplifier uses a p-channel input MOSFET and a MOSFET in the deep ohmic region to form a high resistance in the feedback loop. The feedback resistance is determined by an external voltage bias on a FET and is adjustable anywhere from several kohms to greater than 10^{12} ohms. The pulse shaping circuit uses an ORNL design CMOS operational amplifier in two stages. This amplifier has integral linearity of order 0.1% within 0.2V of each supply rail and was chosen to minimize integral non-linearity due to the shaping network. The shaping poles are provided by n-well resistors with values well into the hundreds of kohms. The shaping is CR-RC^2 with the preamplifier output load providing one pole. The measured linearity, shown in Figure 1, is approximately ± 0.6% of the full dynamic range. The preampifier has a conversion gain of $\sim$11 mV/fC. Each channel (preamplifier and shaping amplifier) dissipates 3 mW power.

The first prototype device has two channels which are identical in most respects except for the input FET gate area. The input FET areas are 2500μm $\times$ 1.2μm and 5000μm $\times$ 1.2μm respectively and were selected to study minimizing noise by trading transconductance *vs.* capacitance. For detectors with low leakage current ($<$ 10 pA) and shaping times $\tau_s < 10\mu$s, shot noise is negligible. Johnson (thermal) and $1/f$ noise predominate. The Johnson noise contribution is proportional to

$$N_J^2 \propto \frac{kT}{g_m \tau_s}(C_{input} + C_{det})^2, \qquad (1)$$

where kT is the temperature, g_m is transconductance, C_{input} is the preamplifier input capacitance, τ_s is shaping time, and C_{det} is the detector capacitance. The *1/f* noise contribution is proportional to,

$$N_{1/f}^2 \propto \frac{1}{C_{input}}(C_{input} + C_{det})^2. \qquad (2)$$

The precise contribution from each noise term is determined experimentally. We expect to be in a domain where the $1/f$ term will either dominate or be roughly equal to the Johnson term. If we were to operate the front end MOSFET in the strong inversion region, then $g_m \sim C_{input}^{1/2}$, and these equations indicate that the minimum noise is provided when C_{input} is in the range $C_{det}/3$ to C_{det}, depending on which noise terms dominate. However, in order to minimize power consumption, we choose to reduce the drain current and operate in the weak inversion region. In weak inversion, the transconductance no longer increases as $C_{input}^{1/2}$, and increasing the FET area no longer provides noise improvement, indicated by Equation 1.

The large gate areas in the design of *NRL-1* provide an input capacitance of 1.5 and 3 pF for channels 1 and 2 respectively, and are selected to be well matched to a detector with capacitance $\sim$10 pF. Noise performance of the chip for both channels is shown in Figure 2. A slight difference in noise was observed, with the smaller FET performing somewhat better.

Optimal pulse shaping was determined using a *Thin Glenn* preamplifier, a predecessor of the *NRL-1*. The shaping time that provides the lowest noise with the *Thin Glenn* (noise corner) is determined from measurements presented in Figure 3. Optimum peaking times are found in a broad range between roughly 6–12 μs. A peaking time of $\sim 8\mu$s was a design requirement for *NRL-1*. The *NRL-1* preamplifier provides one pole in the pulse shaping, therefore, increased detector capacitance increases the peaking time. The slope of the peaking time *vs.* detector capacitance curve is 59 ns/pF. Combined with a 33 pF detector, the effective peaking time is 9.4 μs. The small variation in peaking time with detector capacitance should not be a significant factor in our application.

The two channels of *NRL-1* share a common silicon substrate (Orbit tiny device with dimensions of 2.4 $\times$ 2.4 $\times$

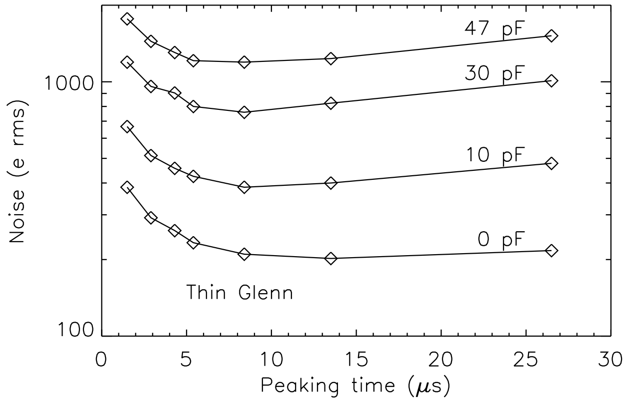

Figure 3: Noise *vs.* peaking time for the *Thin Glenn* preamplifier. The *Thin Glenn* is nearly identical to channel 1 of *NRL-1*, except for a somewhat higher bandwidth. These measurements established the optimum peaking time used in the shaping amplifier stage of *NRL-1*.

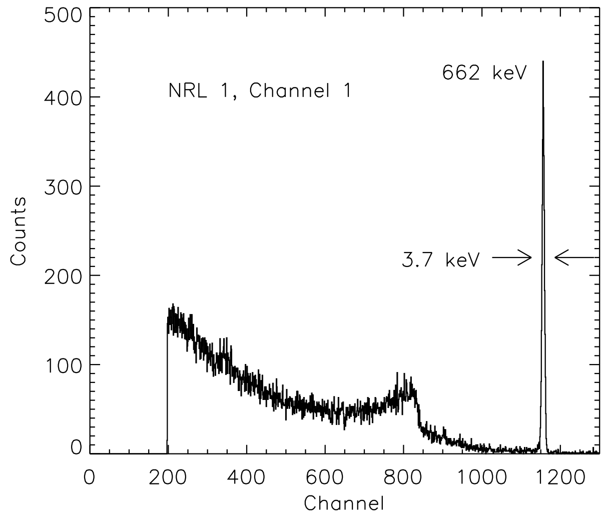

Figure 4: Energy spectrum using one strip from a germanium strip detector and channel 1 of *NRL-1*. A uniform illumination of 662 keV gamma-rays was used. Detector and parasitic capacitance to ground in this system is 33 pF. The peak width is electronics-dominated and is consistant with the noise measurements presented in Figure 2.

0.5 mm). Substrate plugging, *i.e.* filling unused space on the die with V_{dd} and V_{ss} lines, was used to help isolate the two channels. Cross-talk between the channels was measured using a pulser into one channel and observing the signal in the other. With full scale output on one channel, the measured cross-talk in the other is less than 0.1%, demonstrating excellent isolation between the channels. The predominate source of cross-talk in a strip detector application will be between the strips themselves, which is typically on the order of 1%.

Spectroscopy using a strip detector with *NRL-1* is demonstrated in Figure 4. The energy resolution we obtain, 3.7 keV full-width at half-maximum (FWHM), should be compared with 2.3 keV obtained using conventional electronics with a room-temperature JFET. The detector used in these tests has a relatively high capacitance (33 pF) due to cabling and signal feed-throughs in the vacuum bulkhead, thereby degrading the noise performance of the amplifiers. We expect that in an improved design detector capacitance can be reduced to 5–10 pF, and the corresponding performance of *NRL-1* should improve to the range 1.8–2.1 keV FHWM.

Noise is further reduced by cooling the CMOS amplifier as shown in Figure 5. Temperature was controlled in an environmental chamber between -40 C and room temperature. Conversion gain was measured with a pulser and 1 pF test capacitance. Noise was measured with no input using a 1 GHz rms oscilloscope. We monitored rms noise and conversion gain as a function of temperature. We note that conversion gain remained constant throughout this testing, independent of temperature. Cooling *NRL-1* to -40 C improves energy resolution by 0.16 keV. The noise *vs.* temperature curve is very linear down to -40 C, and we expect that further cooling will continue to reduce the noise.

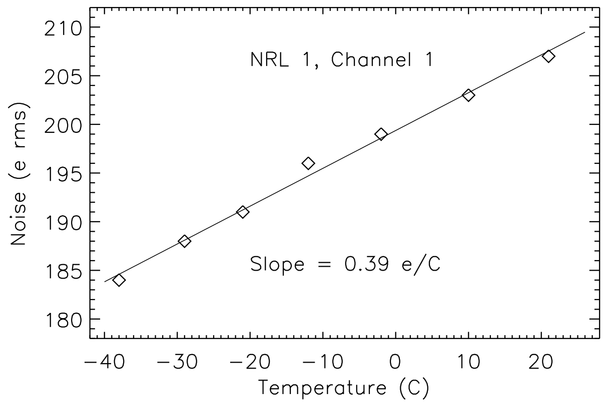

Figure 5: ENC measured for channel 1 of *NRL-1* as a function of device temperature with a 1 pF capacitive load. Measurements were made with both increasing and decreasing temperature to ensure accuracy of the results. If the noise slope continues to 100 K, a potential improvement in energy resolution of 0.5 keV FWHM would be possible.

A new amplifier chip, called *NRL-2*, has recently been fabricated and is now under test. It has a conversion gain 4 times that of *NRL-1* and a dynamic range to ~1 MeV. The higher gain is expected to reduce the electronic noise to ~160e according to HSPICE modeling. Note that HSPICE device models are adjusted to properly compute the actual noise observed in *NRL-1*. The lower noise of *NRL-2* is expected to improve energy resolution by 0.3 keV compared with *NRL-1*.

NRL-2 is part of a complete CMOS spectroscopy system which includes a self-gating analog-to-digital chain for gamma-ray spectroscopy, consisting of three chips: a two-channel preamplifier/shaping amplifier, a two-channel peak detect/sample-and-hold, and a six-channel 12-bit ADC. This spectroscopy system will be the subject of another paper.

III. Conclusions

The current generation of CMOS amplifiers may already be adequate for many astrophysical applications, providing ~2 keV FWHM performance over a wide energy range to 3.8 MeV when used with germanium detectors $\leq$ 10 pF. Further reduction in noise is anticipated using devices with a reduced dynamic range, or by packaging the preamplifiers inside the vacuum cryostat to further reduce detector capacitance, or by cooling the electronics.

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