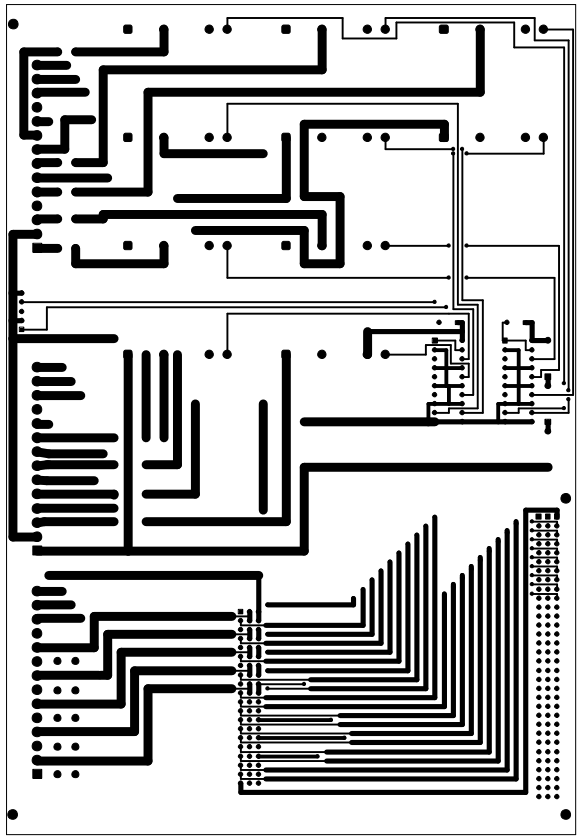
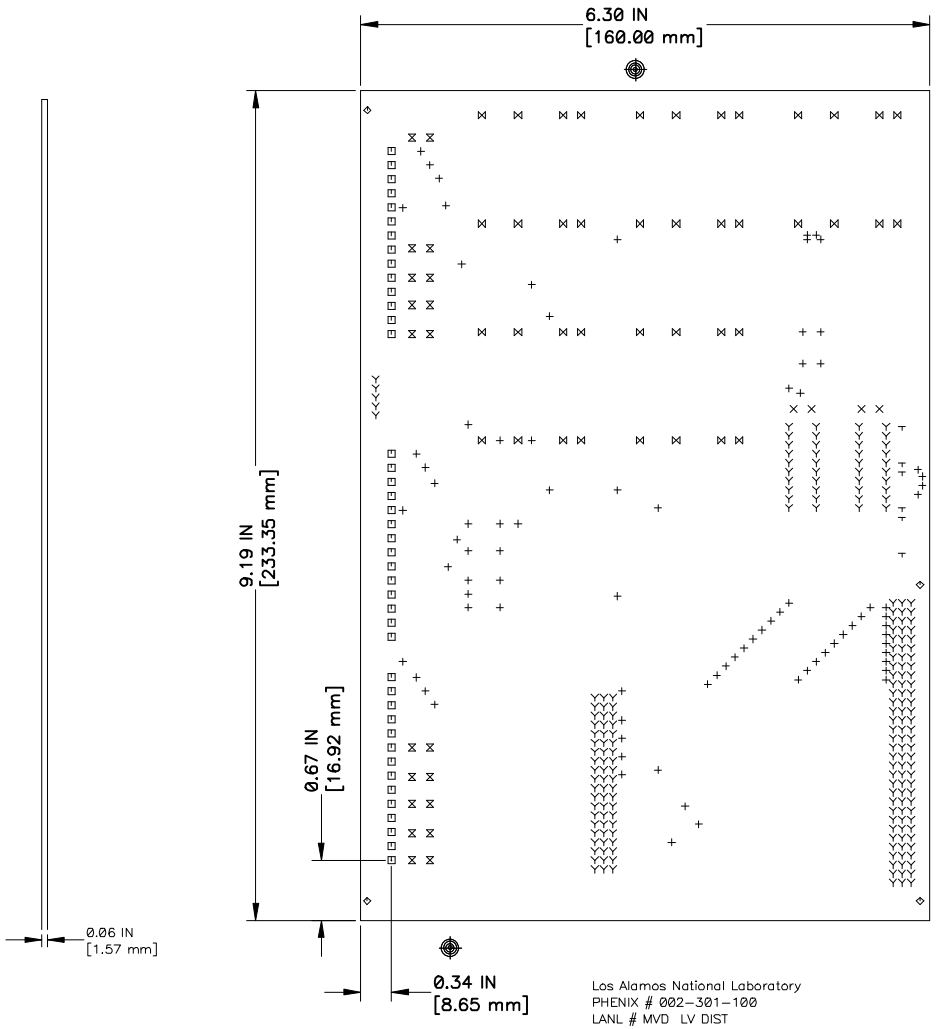


Los Alamos National Laboratory
PHENIX # 002-301-100
LANL # MVD LV DIST
7 June 1999
Bottom Side, Layer 2

Los Alamos National Laboratory		
Title	MVD LV Distribution VME Module	
	PCB	
Size C	Date Originated: 26 May 1999	
	Date Last Revised: 7 June 1999	
LANL DWG # MVD LV DIST VME		Approved By: Boissevain
PHENIX DWG #: 002-0301-100		Drawn by: G. Hart
Filename mvd lv dist vme.pcb		Sheet of



Drill File: MVD LV DIST VME.DRL

Drill Symbol Table			
Hole Dia (inch)	Symbol	Quantity	Plated
0.018	+	87	Yes
0.022	X	4	Yes
0.038	Y	201	Yes
0.046	T	6	Yes
0.048	hourglass	20	Yes
0.058	square-X	40	Yes
0.067	square	42	Yes
0.110	diamond	4	No

1. Board material to be FR-4
2. Final board thickness to be .062" +/- .005"
3. Suface finish: Solder Mask over Tin/Lead
4. All tolerances to be +/- .005" unless otherwise stated.
5. 1/2 oz Cu
6. NC Drill data: Units=Inches, Code type=ASCII None, 0 Supression=leading

GERBER FILES:
MVD LV DIST VME.FAB Fabrication details
MVD LV DIST VME.L1 Layer 1, traces
MVD LV DIST VME.L4 Layer 2, traces
MVD LV DIST VME.SMK Layer 1&2 Solder Mask
Output units=Inches, Numeric=4,4, RS-274-X

Los Alamos National Laboratory
PHENIX # 002-301-100
LANL # MVD LV DIST
7 June 1999
Fab Drawing

Los Alamos National Laboratory		
Title	MVD LV Distribution VME Module	
	PCB	
Size C	Date Originated: 26 May 1999	
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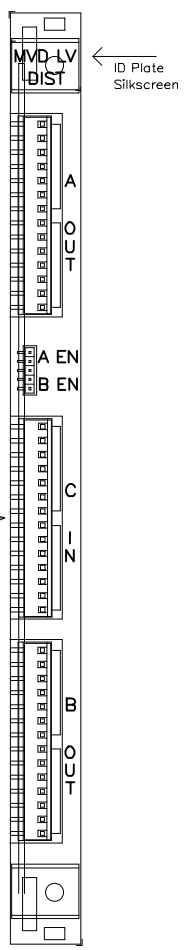
LANL DWG # MVD LV DIST VME		Approved By: Boissevain
PHENIX DWG #: 002-0301-100		Drawn by: G. Hart
Filename mvd lv dist vme.pcb		Sheet of

ITEM	REF #	QTY	MANUFACTURER	DESCRIPTION	PART #
1	P2	1	ITT–Canon	96 pin DIN RA, rows a & c filled	905–72205E
2	P3–5	1	Molex	Header, Right Angle, .156" pitch, 14 pin	41792–0540
3	P6	1	Samtec	Header, Right Angle, 5 pin	TSW–105–08–S–S–RA
4	JH1	1	SAMTEC	Header, 3 row x 20 pin (60 total)	TSW–120–07–G–T
5		1	SAMTEC	Jumper, 20 pair	MNT–120–BK–G
6	RY1–10	7	Crydom	SS Realy, 10 amp	CMX60D10
7	R1–2	2		Resistor, 1/8 w, 10 k	
8	D1–3	3	Motorola	Diode, 1 amp, 600V	1N4005
9	F1–10	10	Raychem	Resettable Fuse, 3 Amp	RGE300

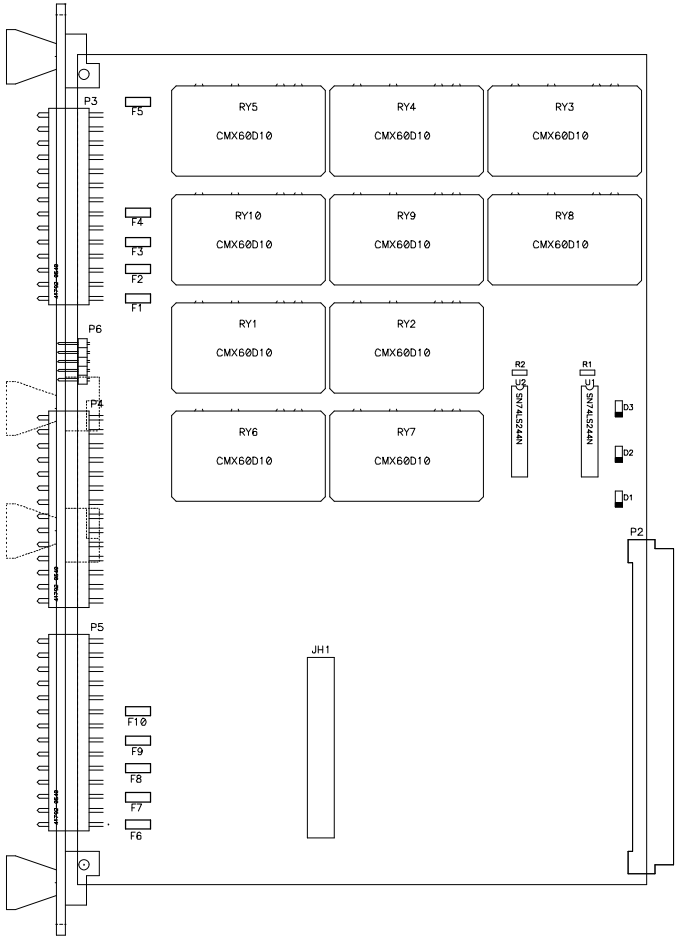
10 mil width traces with 1/2 0z plating = 6 amps
10 mil width traces with 1 0z plating = 12 amps
20 mil width traces with 1/2 Oz plating = 12 amps

Los Alamos National Laboratory
PHENIX # 002–301–100
LANL # MVD LV DIST
ID Plate Silkscreen
Gregory Hart 505–665–0365
ghart@lanl.gov

Los Alamos National Laboratory
PHENIX # 002–301–100
LANL # MVD LV DIST
Front Panel Silkscreen
Gregory Hart 505–665–0365
ghart@lanl.gov

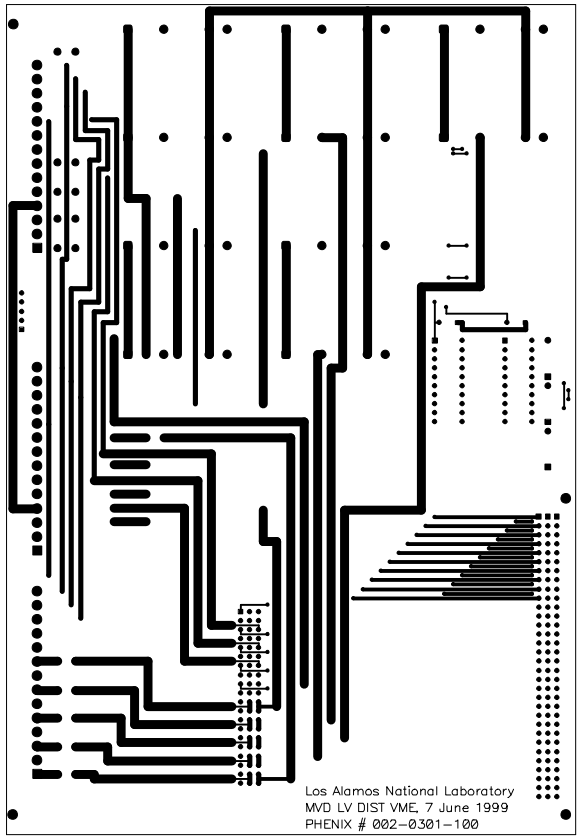


Shown with mating plugs installed



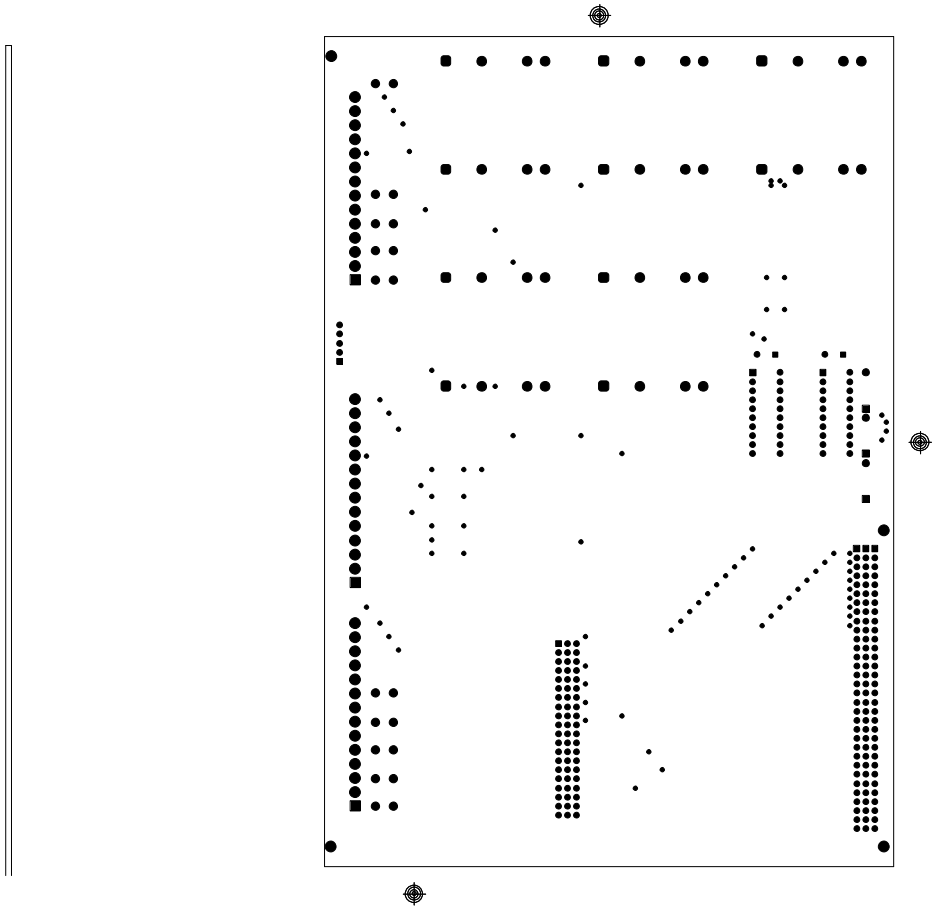
Los Alamos National Laboratory
PHENIX # 002–301–100
LANL # MVD LV DIST VME
7 June 1999
Assembly Drawing

Los Alamos National Laboratory		
Title	MVD LV Distribution VME Module	
	PCB	
Size C	Date Originated: 26 May 1999	
	Date Last Revised: 7 June 1999	
LANL DWG # MVD LV DIST VME		Approved By: Boissevain
PHENIX DWG #: 002–0301–100		Drawn by: G. Hart
Filename mvd lv dist vme.pcb		Sheet of



Los Alamos National Laboratory
PHENIX # 002-301-100
LANL # MVD LV DIST
6 June 1999
Top Side, Layer 1

Los Alamos National Laboratory		
Title	MVD LV Distribution VME Module	
	PCB	
Size C	Date Originated: 26 May 1999	
	Date Last Revised: 7 June 1999	
LANL DWG # MVD LV DIST VME		Approved By: Boissevain
PHENIX DWG #: 002-0301-100		Drawn by: G. Hart
Filename mvd lv dist vme.pcb		Sheet of



Los Alamos National Laboratory
PHENIX # 002-301-100
LANL # MVD LV DIST
7 June 1999
Solder Mask, Layer 1 & 2

Los Alamos National Laboratory		
Title	MVD LV Distribution VME Module	
	PCB	
Size C	Date Originated: 26 May 1999	
	Date Last Revised: 7 June 1999	
LANL DWG #	MVD LV DIST VME	Approved By: Boissevain
PHENIX DWG #:	002-0301-100	Drawn by: G. Hart
Filename	mvd lv dist vme.pcb	Sheet of