

# Technical Review Committee Meeting

*June 10-12, 1998*

Review of PHENIX Front End Electronics

Reviewers: Richard Jared (LBNL), Andrew Lankford (UC Irvine, Chair), Ed Obrien (BNL), Renee Poutissou (TRIUMF), Veljko Radeka (BNL), Sergio Rescia (BNL), Richard Van Berg (Pennsylvania)

Also Attending: Thomas Ludlam (BNL), Alan Stevens (BNL)

## **I. Executive Summary**

The purpose of this review was to examine the status of the PHENIX Front End Electronics (FEE) with special emphasis on potential problems regarding readiness for Day 1 physics in October, 1999. The letter giving the charge to the review committee is attached to this report as Appendix 1, and the agenda for the review as Appendix 2.

Progress on PHENIX FEE has been significant, and the rate of progress continues to improve. Subsystem designs are all nearly complete. Some ASICs are in production or have completed production. All ASIC prototypes have integrated full functionality. Many board designs have reached the prototype phase. A few boards are in production or ready for production. The common electronics is largely complete and ready in time for use by FEE subsystems. Several successful chain or system tests have been accomplished. Plans and schedules are coherent, if aggressive. The level of effort has been greatly strengthened. Nevertheless, areas of significant technical risk remain, particularly in subsystems that have not yet completed system tests, and schedule risk is widespread. Progress must continue to accelerate in order for completion in time for the Engineering Run and Day 1 physics.

PHENIX has successfully addressed nearly all the recommendations of the November 1996 review. In particular, tremendous progress has been accomplished on pad chamber readout, on system and board designs, on common electronics systems such as timing and control, and on partial chain tests. Manpower and management concerns expressed in that review were also addressed.

### Schedules

Although enormous progress has been accomplished since the last review, the pace of progress must continue, or even quicken, in order to meet the aggressive schedules of most subsystems. Much work remains, not only in completion of the fabrication of the subsystems, but in commissioning the subsystems and in integrating the subsystems into PHENIX as a whole.

## Chain/System Tests

Significant technical risk remains until the completion for each FEE subsystem of chain/system tests that demonstrate required analog performance in the presence of simultaneous digital activity. Plans for such tests exist for all subsystems. These tests should continue and expand. They should grow to incorporate enough channels to ascertain that the system can be scaled without inducing oscillation or other coherent problems. They should also incorporate low voltage power supplies and cables of the final design. Chain tests for each subsystem should transfer formatted data into a DCM under control of the timing system.

## Electronics Coordination

Electronics coordination has been strengthened significantly since the last review. Nevertheless, the scope of this activity for a detector as diverse and technically challenging as PHENIX demands that the electronics coordination be broadened. For instance, an additional person could be appointed to coordinate infrastructure and support, and another person could be appointed to coordinate the integration of FEE systems with common electronics such as DCMs, timing, and controls. These coordinators would work with the Deputy Project Director for Electronics in order to assure the timely completion of the electronics during this period of rapidly growing activity.

## Principal Recommendations

We list here the issues and recommendations stemming from this review that deserve the most immediate attention:

- (1) As discussed immediately above, in order to broaden the electronics coordination effort and to prepare for a rapid growth of activity during the testing and commissioning phase, PHENIX should augment the electronics coordination team.
- (2) Although no immediate action is needed, the MVD multi-chip module (MCM) is near the critical path. Careful attention should be paid to the milestones mentioned in the discussion below.
- (3) The Muon tracking system, consisting of both detector and readout electronics, should be re-examined by the PHENIX collaboration in the context of global optimization of detector performance and electrical/mechanical design.
- (4) Design of grounding and cooling for the Pad Chambers must be completed in time to affect PC mechanical design if necessary. A workshop or task force approach to resolving these issues on the time scale of a month is suggested.
- (5) The schedule for Level 1 trigger design and production is overly aggressive. PHENIX should reevaluate the proposed schedule for delivery of trigger boards, considering possible delays in design or production, in order to reorder priorities or augment the Level 1 development effort as needed.

Elaboration on these issues, as well as additional concerns and recommendations of the review committee, are given in the remaining sections of this report.

## **II. MVD**

The Multiplicity/Vertex Detector is a compact, self-contained subsystem that will be installed after most of the detector has been completed and the machine operating conditions have been well established (to prevent damage to silicon detectors). The mechanical and thermal design are based on a solid expertise in this area available at LANL.

Due to the high segmentation of silicon detectors, the readout has to rely on high density interconnects and packaging. The proposed technology for the multi-chip modules (MCMs) is among the most advanced, but very demanding with respect to complete die testing, accuracy of layout, and quality control at every step of the process.

Significant progress has been made in various aspects of the overall subsystem and in preparation of the facilities and testing of the MVD. Essentially, all readout components have been designed and the prototypes fabricated.

The MCM remains the critical component and is clearly on the critical path for the overall schedule. Any iteration in the MCM will have a large effect on the schedule. In the development of this module, it is encouraging that a good communication has been established with Lockheed-Martin unit fabricating the MCM.

There are two near milestones that should clarify most uncertainties with respect to the MCM:

1. Analog input tests on the printed circuit version should be completed in the next two to three weeks. Noise measurements should be made (taking into account different lead lengths and capacitances). An input dc current equal to the maximum expected detector leakage current should be injected into the input in order to test the behavior of the input ASIC. The results of this test should be reported to the PHENIX Electronics Coordinator promptly.
2. The pre-production MCM is due in September. Crucial tests of the performance will have to be completed in a very short time (3-4 weeks). The final design review will have to be performed at this point (Oct. 1998).

## **III. TOF, Beam-Beam**

### (A) Time of Flight

The Time of Flight (TOF) subsystem is based on a tested design (which has been used in the experiment WA98). About one half of the subsystem has been completed. The subsystem is expected to be ready when the experiment is turned on.

## (B) Beam-Beam Counters

The completion of this relatively small subsystem is planned by the end of this calendar year and there appear to be no technical or scheduling problems.

### **IV. Drift Chamber**

The Drift Chamber system has continued to make good progress and is approaching a complete final design. The integrated circuit components are all in hand, the prototype front end boards have been shown to work in a reasonably realistic environment—meeting or exceeding the PHENIX requirements for both efficiency and resolution (although tests at realistic hit rates and particle densities remain to be carried out). The major remaining issues center around systems level integration questions such as cooling and cabling and should be largely or entirely answered in the upcoming round of prototype tests. None of the remaining questions seem fundamental; the chamber team seems to have the tasks well in hand and the implementation of the DC FEE system seems to be proceeding smoothly and competently. However, as with all the PHENIX systems, the schedule is tight and production and testing of the complete system will require a large and concentrated effort at the end of this year if the schedule is to hold.

### **V. Time Expansion Chamber**

The Time Expansion Chamber has also demonstrated good progress and is also at a nearly complete and final design for the electronic system. The performance of the chamber-electronics system is excellent; the integrated circuit designs are complete and large quantities of all chips are on hand or will be available in a few weeks. The preamp- shaper board is production ready and a prototype FEM board has demonstrated the required performance. There seem to be no outstanding fundamental problems with the system or its implementation and the design team seems to be competent, enthusiastic, and fully capable of carrying the project to completion. Nevertheless, there are a few areas that should continue to receive attention. The full 64 channel FEM card needs to be completed and tested in a timely manner. The tested 64 channel FEM will allow a full set of chain tests to be carried out. We note that the total number of fairly complex cards (the P/S and the FEM) required by May of 1999 is not so small and the testing plans are very aggressive - especially given that a full chain test is not planned to take place until December 1998 so that production of the full number of boards can not start until 1999.

## **VI. EMCAL**

The EMCAL FEE has made good progress since the last review, but there still is work to do. The project contains three ASICs, five varieties of custom circuit boards and a custom backplane. One area where the project has made great strides is in the level of scientific manpower. A major concern at the last review was the small number of physicists involved in the EMCAL FEE. Manpower needed to be increased and responsible physicists needed to be identified. The EMCAL group has done a good job addressing these concerns and they are no longer considered significant issues.

The plan to complete the EMCAL ASICs looks reasonable. One of the three EMCAL ASICs, the AMU/ADC, has its design completed and has been fabricated. It is shared with other subsystems. The two INT chips, one for the Pb-glass and one for the Pb-Scintillator, are still being prototyped and require a number of fixes. The group acknowledges that one could go to production with this chip, but with performance limitations in the timing resolution. The collaboration should decide soon which way to proceed. PHENIX currently favors doing one more round of prototyping in combination with the RICH-INT to bring the chip within specifications.

The EMCAL Front End Module (FEM) is actually ten circuit boards of five varieties plus a custom backplane. Prototypes exist for some of the boards but the most challenging ones, the ASIC and Trigger boards, are not yet complete. First prototypes of these are to be ready for testing within the next few weeks. Once the ASIC boards are complete, priority should be put on testing the INT and AMU/ADC chips together on the same board. This is an important outstanding issue. The plans for system tests of the FEM appear to be limited. FEM prototype testing should include thorough tests of a full FEM system, including attachment to as many EMCAL supermodule channels as practical. One QA issue that should be considered is whether the FEM boards have enough diagnostic features in their design. Board troubleshooting can become difficult in multi-board systems with inconvenient access. We also note that the time allocated in the EMCAL FEE plan to produce and test the required 2200 boards assumes a very aggressive schedule.

## **VII. RICH**

The RICH FEE has significantly increased the manpower associated with the project. Increased participation by the University of Tokyo group, together with new groups from Waseda Univ. and Nagasaki Institute of Applied Science, should provide the project with sufficient resources to allow a successful completion.

Of the two RICH ASICs one is produced and one is yet to be prototyped. The AMU/ADC is fabricated and is being packaged. The RICH INT chip, which has not yet been prototyped, is very similar to that of the EMCAL INT with less stringent performance requirements. The PHENIX

plan to fab the RICH-INT chip after one round of prototyping would normally be seen as too optimistic, but may be possible considering the design overlap with the EMCal INT which has been through prototyping stages.

The RICH FEM is a custom crate-based design containing five types of printed circuit boards and a custom backplane. The cards are in various states of design with the exception of the preamp card which is in production. The RICH FEM boards have many of the same issues of concern as is the case in the EMCal subsystem. The RICH group should plan a complete FEM system test with a significant channel count as part of their prototype tests. The tests should include actual elements of the detector. The sufficiency of the FEM board diagnostics should be examined. The RICH FEM schedule shows three prototyping rounds for each board. With carefully planned design reviews and close communication with the ORNL group, one may be able to eliminate a prototyping round and so gain schedule contingency.

### **VIII. Muon ID**

The PHENIX Muon ID detector has showed a great deal of progress, especially considering the late start on this subsystem. The pressure to meet the detector deployment schedule, however, forced some decisions which might affect the long term performance. No burn-in of the inaccessible in-panel preamplifiers is currently being performed. (The 24-hours power on test will not weed out the "infant mortality"). While it is too late for the panels already installed, it might still be possible to perform more extensive room-temperature burn-in in the factory while the preamplifier PC boards are being installed on the detector. All the FEM and ROC functionalities have been established at the block diagram level. Many subsystems (ARCNET etc.) have been already designed for other PHENIX detectors and can be used with minor modifications, thus simplifying the design effort and minimizing the risk. The ROC board is a high density (96 channels), mixed signal board with multiple sets of 96 lines routed throughout. It is important to dedicate enough time and effort in the 8 channels prototype to test the design and the interactions of the different components. It will also be essential to use the full board in the chain test with the detector before proceeding with full production and procuring all components.

### **IX. Muon Tracker**

Like the Muon ID, the PHENIX Muon Tracker electronics effort has suffered from a late start and lack of (or delayed) funding.

The charge sensitive preamplifier has been tested, but a more careful characterization is necessary. In particular the non-linearity, a very important specification for a system which uses linear interpolation, must be fully understood. A poor non-linearity in the lower portion of the

dynamic range was noted. A chain test with more than 8 channels which exercises all the functionalities (calibration etc.) should be performed before proceeding with procurement.

The late start is reflected in the current status of the readout system and dictates the schedule. A better planning of the grounding and understanding of the flow of signal currents is necessary. A chain test with a suitable number of channels (64 or more) should be performed to test the readout architecture and to verify the performance of the detector-readout electronics system and should be a high priority item.

The system as it was described in this review seems unnecessarily complicated. The entire system of detector and readout electronics should be re-examined by the PHENIX collaboration in the context of global optimization of detector performance and electrical/mechanical design. The constraints of the detector (mechanical stability, acceptance angle, etc.) on the electronics seems overly demanding and forces more complex, costly and risky solutions on the electronics design and assembly, possibly compromising performance and robustness. By marginally relaxing detector requirements it might be possible to streamline and simplify the electronics and ultimately design a more robust system. An example could be the present CAIC and CROC boards which forces low level signals through three boards and multiple sets of connectors because of the space constraints. By relaxing those constraints it might be possible to streamline the design in a single board which minimizes the risks of signal degradation and electromagnetic interference pick-up.

## **X. Pad Chamber**

The Pad Chamber Group has made good progress since the last review. A successful reorganization has taken place resulting in a team that is coherently addressing issues and has identified most outstanding items. At the present time the principal outstanding issues are grounding paths in the chamber, cooling of front end electronics, a residual problem in ASIC design, and quality assurance.

The most significant items (grounding and cooling) are those that may affect the mechanics of the chamber. Currently, safety issues associated with the adjacent RICH chamber require that the Readout Cards (ROCs) must be in a nitrogen atmosphere. The use of forced-flow nitrogen gas as the method to remove the heat would not be sufficient in the current design, with the likely consequence that heat from the front-end electronics must be removed by conduction. The only readily available metal at present (and metal must be minimal) is the ground plane for the pad chamber. Use of this surface would require that it be cooled by some method (water., heat pipes, etc.). There was no specification available on what the temperature of the pad chamber must be, which must be addressed when determining the cooling system. The second cooling issue is the Front-End Module (FEM) on the end of the chambers. This area is easier to cool but a plan must be completed to provide this cooling function. Grounding of the chamber (i.e. the complete signal

path) was not completely described. It is also noted that the front end electronics threshold tests showed changes in threshold (assumed due to grounding problems) between two front end card boundaries. The effect was of a magnitude that used most of the margins in the electronics specification, which in turn could jeopardize the physics performance if the effects are larger than shown. This may be an artifact of the testing system, but is considered to be a significant concern. Both of these issues (grounding and cooling) could affect the mechanics of the chamber. It is recommended that Pad Chamber Group find solutions to these concerns in a short period of time, perhaps four weeks, which may require workshops and/or other group meetings that span both mechanics and electronics. The result of this effort should be planned solutions backed up by calculations. The effect on the mechanical system must be understood in a timely fashion, in order that any necessary chamber design changes can be prototyped and tested, and that chamber design can be finalized. Tests should show that the electronics performs to specifications with the mechanics of the chamber and that heat is properly removed.

The current ASIC has a problem with the discriminator level drifting with a time constant of a few hours. This problem (which is not completely understood ) must be corrected in the next iteration or the schedule will slip.

Quality assurance issues for the pad chamber electronics are reliability and allowable bit error rates. The PC1 and PC2 chambers are very difficult to access, which results in a premium on reliability. It is recommended that FEM and ROC cards be burned in to the extent possible to improve their reliability. There were no plans to establish criteria for system performance. It is recommended that effects of bit error rates be analyzed and measurements be performed during the system test (before the final design review) to establish that error rates are below the threshold of concern.

The schedule is aggressive and the pad chamber needs to be installed for day one running. An aggressive schedule is good, but milestones need to be reviewed and then tracked carefully. New milestones should be added to cover grounding and cooling.

## **XI. DCM, Level-1**

### **(A) DCM**

The Data Collection Module (DCM) main board and its compressor daughter cards have been designed and tested. The DCM passed a Final Design Review in January 1998, and has completed chain tests with the Timing System and the Front End Modules (FEMs) of two subsystems. It will be released for production as soon as a chain test is completed with its crate backplane and partitioner card. The DCM partitioner card is presently under test. Parts for DCM

production have been ordered. Production could be complete by the end of the year, well in time for the needs of front end electronics subsystems and DAQ.

### (B) Level-1 Trigger

Detailed design of boards for the Level 1 Trigger has begun in earnest. A prototype of a TOF LL1-2 type board is now under test. The team of physicists involved has grown quite markedly in the past year.

Altogether Level 1 consists of 92 large format boards of 16 different types and 86 transition cards of 5 different types. Design of this many boards in a short period of time is a daunting task. A plan has been defined to complete and commission trigger boards in the order and at the time they are needed for physics, starting with the GL1, BB, and MVD for Day 1 physics. Although many design blocks will be shared by many board types, the completion and production of this many designs, as well as integrating and commissioning the full system, within a short two year period is overly optimistic. Digital boards of this variety require substantial time for design verification both by board level simulation (including timing) before fabrication and by extensive testing to provide adequate fault coverage after fabrication. PHENIX should evaluate the proposed schedule for board deliveries in light of possible delays, in order to reorder priorities or augment the Level 1 development effort as needed.

The EMCal trigger would be needed by early physics with other than minimum bias triggers in the unhappy event that the MVD was not ready to go on the beamline. Consequently, development of the EMCal trigger must be kept on its planned schedule for completion in late 1999.

## **XII. System Integration, Timing, Quality Assurance**

### (A) Electronics Infrastructure

The design for the low power distribution system appears adequate. It is really a suite of commercial modules repackaged to suit the footprint of PHENIX. It includes all available hooks for monitoring and interlocks. Integration in an overall slow control system using EPICS is planned, but no real estimate of the scope of that work has been made. The High Voltage systems, of which there are 3 kinds from different manufacturers, will be controlled by EPICS.

Other detector groups have successfully used EPICS for this purpose but management should be aware that this has been quite labor intensive. It would be wise to make it someone's main priority.

Installation of electrical services in the counting room and hall is behind schedule, but it is hoped that proper priority to this job will be given in time for testing of detector prototypes due to appear in the next few weeks.

The committee had some concerns about a lack of overall plan for power up operations. Each subsystem should be aware of what state their electronics will be in after power up. Such a plan should assume that ARCnet might not be operational. It should also give specifications on constraints for sequence of power turn on, etc.

FPGA loading is also a concern. Some questions which should be asked and answered are: Is there a sequence needed, where will the load files reside, how long will it take to bring up the whole detector?

#### (B) Event Synchronization

There is a mechanism in place to send a reset signal to all timing granules. From that point on, each subsystem adds time stamps to the data flow. The Level-1 also adds its own time stamps. The DCM are the first modules in the chain to check the consistency of these time stamps. What to do in case of errors seems an unresolved issue that needs attention. It might be indicative of what appeared to the committee to be the lack of a clear interface between the DCM, the event builder and ONCS. This is a matter that needs attention but that is beyond the scope of this review.

Overall handling of errors and what to do when an error is detected is not well specified at the present time. This ties in with the general issue of Quality Assurance elaborated below.

#### (C) Timing and Controls

The main functions of the timing system appears to be well in hand. ARCNET cards are available and in use. The committee sees no problems in this area.

#### (D) QA

Final design reviews, which are considered by the Collaboration equivalently as pre-production reviews, are an essential step to ensure proper functioning and reliability of all the subsystems. It is important that these reviews include a detailed QA plan. As noted in some of the earlier sections of this report focussed on the various subsystems, it is clear that not much attention has been devoted to burn-in procedures for electronics. Burn-in procedures should be determined from the requirements on reliability of particular components, the effect of their failures on the performance of the experiment, and the access for replacement. Final design reviews of all ASICs prior to production is a necessary part of the QA process.

The existence of a documentation system for electronics for the whole experiment was not evident from this review. A documentation system, with some reasonable hierarchy (distinguishing items of common concern from detailed board-level documentation), would aid in QA, reliability and safety of the equipment as well as in maintenance during operation. Some items in the

"common" category are grounding and shielding, power supplies, interlocks, fire protection of electronics, power dissipation and heat removal.

## Appendix 1

## Appendix 2

### PHENIX FEE/Online Review Agenda

Bldg. 1005, Third Floor Conference Rm., Brookhaven National Laboratory  
June 10 - 12, 1998

#### Wednesday, June 10

8:30	a.m.	Committee Executive Session		(30)
9:00		Overview	S. Aronson	(20)
9:20		ASICs Status	G. Young	(30)
9:50		System Design Status	J. Haggerty	(30)
10:20		<i>Break</i>		(15)
10:35		The Thin Glenn Preamplifier-Discriminator and AMUADC chip	C. Britton	(20)
10:55		EMCal/RICH ASICs	A. Wintenberg	(20)
11:15		TEC ASICs	P. O'Connor	(20)
11:35		PC ASICs	W. Bryan	(30)
12:05	p.m.	MuTr Cathodes Preamp Status	M. Musrock	(15)
12:20		<i>Lunch</i> (Working)		(1:10)
1:30		Electronics Infrastructure	S. Boose	(40)
2:10		Timing System Main Functions	J. Mead	(20)
2:30		DCM Review, Fab. Plans, Chain Tests	C.-Y. Chi	(20)
2:50		<i>Break</i>		(15)
3:05		PHENIX Level-1 Trigger	J. Lajoie	(40)
			F. Wohn	
3:45		BB/TOF FEE	C.-Y. Chi	(20)
4:05		MVD		(40)
		Status of ORNL Interface Boards	S.-K. Hahn	
		MVD Electronics	J. Simon-Gillo	
4:45		DC FEE	T. Hemmick	(20)
5:05		Committee Executive Session		
7:30		Committee Dinner		

#### PHENIX FEE/Online Review Agenda (Continued)

#### Thursday, June 11

8:30	a.m.	Committee Executive Session		(30)
9:00		PC		(40)
		FEM Status & Plans	M. Smith	
		Schedule, Testing, Installation	H.-A. Gustafsson	
		PHENIX Pad Chamber FEE	V. Greene	
9:40		TEC		(30)
		Electronic Manpower	S. Rankowitz	
		Schedule, Testing, Installation	R. Seto	
10:10		<i>Break</i>		(15)
10:25		EMCal		(40)
		Boards	A. Wintenberg	
		Schedule, Testing, Installation	P. Stankus	
11:05		RICH	K. Oyama	(30)

11:35		<i>Lunch</i>		(1:25)
1:00	p.m.	MuID		(30)
		Boards, Prototype Status, Timeline	M. Rao	
		Schedule, Testing, Installation	V. Cianciolo	
1:30		Muon Tracker FEE	B. Wong-Swanson	(40)
2:10		<i>Break</i>		(15)
2:25		Integration/Installation at BNL	J. Haggerty	(50)
3:15		Discussions with Collaboration as Needed	(1:00)	
4:15		Committee Executive Session		
<b><u>Friday, June 12</u></b>				
8:30	a.m.	Committee Executive Session		(30)
9:00		Further Discussions with Collaboration As Needed		(1:00)
10:00		Committee Executive Session/Report Writing/Lunch		(3:30)
1:30	p.m.	Close Out		
2:30		Adjourn		

**Review Panel:**

R. Van Berg (Pennsylvania), R. Jared (LBNL), A. Lankford (UC Irvine, Chair), E. Obrien (BNL), R. Poutissou (TRIUMF), V. Radeka (BNL), S. Rescia (BNL)