PHENIX Internal Review
of the FPHX Chip Testing
5-March-2009

A preliminary review the status of the FPHX testing was conducted on March 5, 2009. In addition to FVTX personnel, John Haggerty, Cheng-Yi Chi and Ed O'Brien from the PHENIX collaboration were present. The goal of the review was to evaluate the status of the testing so far completed and consider what additional testing was required prior to starting the redesign of the FPHX chip.

Two presentations were made by the FVTX groups. The first, by Jon Kapustinsky, focused on the analog tests done on the chip. The second presentation was presented by Sergey Butsky and focused on the tests of the digital back end. Both presentations are posted to the PHENIX FVTX CDS agenda page and the VTX/FVTX TWiki.

The FPHX chip is designed as a fully functional 128 channel silicon strip readout chip with a 3 bit ADC. The chip design was optimized for the FVTX silicon strip sensor design. The design of FPHX prototype chip included spy pads that allow for the observation of the analog signals in the front end. In, addition, the first 15 channels of the chip were designed with different W/L combinations for the input transistor to allow for the optimization of the W/L.. The chip has a large number of programmable features (e.q. Bandwidth, gain, comparator thresholds, etc) that allow for flexibility in its use.

The testing done and reported on has involved 2 FPHX chips mounted on separate test fixtures. One test board is at LANL and the other at FNAL. The readout of the FPHX chip is done by a dedicated test stand designed for specifically for testing the FPHX chip. The test stand allows for full control of all digital components of the chip, injection of an analog pulse into the FPHX analog inject and read out of the FPHX chip at the full design readout speed. The mounting board for the FPHX test was a modified board used for another project and includes decoupling capacitors, and termination resistors for the LVDS signals. Power (+2.5V Analog, +2.5V Digital) is provided by linear power supplies with no voltage regulators on the test board.

Most of the detailed analog studies presented were done by Tom Zimmerman at FNAL. The studies focused on the analog front end and done by looking at the signal response for different programmable features. The results shown were a subset of the full measurements, but sufficient to show that the front end analog section operated as designed and there were no fundamental problems with the analog design. Based on the noise measurements for the first 15 channels of the chip, Tom has selected the optimal W/L for the input transistor which will be implemented on all 128 channels in the next round of the design.

The testing of the digital back end has been done primarily at LANL with some additional studies and verification done at FNAL. The studies have included: reading and writing all registers in the FPHX chip, reading data out at full speed, masking off various channels and reading out unmasked channels, performing threshold scans and calibration studies, looking at the stability of beam clock counter and the phase sensitivity of the reset. For many of the digital operations, no details of how the tests were done were presented, only that they had been tested and the chip performed as expected. Details were presented on the threshold scan, calibration studies and timing studies of an input pulse with respect to the phase of the clock. The results of the calibration and threshold scans indicate that the chip is working as designed. However, the timing studies did uncover one problem with latching of the beam clock that gives rise to hits being assigned the wrong BCO. Jim Hoff has looked at the logic, and has identified a weakness in the logic, which he believes can be fixed in the next design round..

Throughout the presentations, comments were made and a number of concerns were raised about the completeness of the testing and further testing that should be done..

It was pointed out that there really are two types of the testing that need to be one, One is from an electrical engineering standpoint which address the functionality of the device under ideal conditions, and the second is how the chip behaves in the real world, that is, as part of detector. Most of the results presented at this review addressed the first type of testing. The FVTX group agreed that there was a need to test the device as part of detector and has plans to do so in the coming months. Prototype HDIs and sensors are either available or will be in the coming weeks and there is a plan to assemble several FVTX wedges to do these type of tests with. Details of the plan and schedule were not presented, however, there was an indication that this would happen in the next 6 to 8 weeks.

There are a number of performance issues that should be tested which may come into play with the HDI. However, it should be possible to make some of these tests with the current test stand. These tests include understanding the drive capability of the LVDS drivers for different settings, and looking at the phase margin between the beam clock and serial clock, and the reset and the beam clock. If possible, there should be some studies of the effects of digital activity on the analog performance of the chip. Studies of the recovery time for the analog front end should also be done by looking at the front end response after a saturating pulse is injected into one or more channels. Finally, chip operations should be verified at the nominal PHENIX BCO frequency of 9.4Mhz, to make sure that there are no unexpected operational issues associated with a frequency shifts in the BCO.

There has not yet been any long term studies done on the chip. Most studies are done over a short time period (1-2 hours) and then the chip is powered off. In regular operation, the chip will have to operate stably for weeks and months. Studies should be done to verify the stability of the chip over longer operational periods.

So far the chip has only been powered by dedicated linear supplies. In real operations, this most likely will not be the case. In addition, in a real detector, there may be voltage drops such that multiple chips will be operating at slightly different input voltages. Studies should be done to understand the chip response as a function of input voltage over a limited range about the nominal operational voltages. Studies should also be done to make sure that there are no issues associated with the slower turn on of the voltages that one might expect from switching supplies.

There was some discussion at the end about the schedule and the pros and cons of doing another MOSIS run, or going straight to an engineering run. The estimate is that there is between 1 and 2 weeks of redesign work for currently known changes followed by 2-3 weeks of simulation work to verify the new design before submission. The goal is make the May 25th MOSIS submission date. There is some concern that this is optimistic given that the chip has not been tested with a sensor on HDI and those tests are still several weeks away. The FVTX group should take a careful look at the implications to both the cost and time schedules for a May submission verses an engineering run that would be done a a later date. This should include a detailed analysis of both the cost and time contingencies associated with the project for both scenarios.

Overall, the tests done to date look encouraging and many aspects of the chip work as designed. There is consensus that more testing of the chip needs to be completed before the next round of redesign is completed and the chip submitted for fabrication. Most of these future tests should focus on how the chip will operate in experimental environment. Once the testing and redesign is complete, there should be another review of the chip testing and design prior to submission.