PHENIX Internal Review
of the FPHX Chip Testing
12-May-2009

A follow up review of the FPHX testing was conducted on May 12, 2009. In addition to FVTX personnel, John Haggerty, Cheng-Yi Chi and Ed O'Brien from the PHENIX collaboration were present. The goal of the review was to evaluate the status of the testing on the chip, consider what additional testing should be done and preparations for submission of the next Mosis and/or engineering run. Discussion of the submission included the impact on cost and schedule.

Two presentations were given by the FVTX group outlining the testing done to date on the Analog and Digital portions of the FPHX chip. This was followed by a 2 presentations from the design engineers, Tom Zimmerman (analog) and Jim Hoff (digital). .

The analog tests were done at FNAL and LANL and reported at the last review. Based on these studies, the conclusion is that the analog front end performs as designed. Looking at the front end performance of the first 14 channels that have different W/L's for the input transistors, the optimum W/L (222/0.6) has been selected.

Additional testing of the chip has been done focusing primarily on the digital back-end and overall chip performance on a single chip test stand, and HDI (flex and PCB) with sensor. New tests reported since the last review focused on the additional testing as suggested at the last review. All of the results are in the posted talks and for the most part, the chip performed as expected.

Studies performed:

1. Power Supply Response: Input voltages were independently varied from 2.5V to 2.0V in -0.1V steps. For the analog voltage, a slow upward trend in noise and threshold was observed. For the digital voltage, the chip started to report wrong BCO values for 20 % of the channels, but this was not reproducible. At 2.2V the BCO was often incorrect and reproducible. Below 2.1V the chip generated large amounts of data.
2. The signal cable was increased to 2m and the report was that there was no change in the signal shape. No data was presented..
3. The pulser signal was increased by a factor of 3 and a shift of the BCO from the expected was reported. Increasing the pulser signal by a factor of 5 increased the data volume significantly with wrong BCO. At present it is not known if this is a problem with the chip or an artifact of the pulser circuit.
4. Several HDIs, both flex and PCB, have been populated with both FPHX chips, and sensors. Tests that have been performed have been limited due to problems with biasing the sensors and interconnect issues with the readout system.
    1. With these assemblies, readout of up to 13 chips on one side of the wedge has been done for calibration data.
    2. Noise studies with the sensor biased have also been performed. The first look at the data looks like the chip is behaving as expected.
    3. There is some question about some noisy channels, and why there are not uniformly distributed.
    4. The noise level looks to be 400-600 electrons, nominal noise level 400 electrons
    5. Expected dependence on input capacitance has been observed.
    6. A number of chip parameters have been investigated and the results reported.

An overview of the changes to the front end portion of the chip was given by T. Zimmerman. These changes include:

1. Implementing optimal W/L for all input transistors.

2. Changing the staggering of the input pads to match the stagger of the pads on the silicon for easier bonding.
3. Modifications to the shaper/comparator design to reduce the threshold dispersion
4. Addition of 1 bit to the integrator gain select to allowing finer gain setting which will allow for improved optimization of trade off between threshold dispersion and dynamic range.

The first 2 changes are trivial and should be straight forward. The change to the W/L was an expected change, given that the first round chip was designed with channels having different W/Ls to allow optimization of the W/L.

The change to reduce the dispersion is more involved due to the source of the dispersion. It will require redesign, simulation and layout of the shaper/comparator portion of the chip. The layout will be larger, but should be accommodated by free space in the digital back-end. It is expected that the changes will decrease the dispersion by 2/3 from the current dispersion. With a gain of 100mV/fC, this translates into a dispersion of about 170 electrons.

The last change should also be trivial since the required bit is already present in the design and only needs to be implemented. The gain range, will be approximately the same, 50mV/fC to 200 mV/fC. At a setting of 150mV/fC there should be a 50% improvement in the dispersion compared to 100mV/fC.

Jim Hoff reported on the t3 changes in the back-end:

1. The freeze-frame problem with the BCO
2. Modifying the serial out selection to allow selecting either or both serial out lines
3. Increasing the number of time bits to 7

The most difficult change was the freeze frame change and was due to the difficulty in identifying the actual source of the problem. Once identified, it was possible to see the error in simulation and develop a solution. Implementation in the chip design is straight forward. Increasing the number of time bits was also a straight forward change. The chip already has a BCO counter with 8 bits, so the change only involves redefining the output word to include the extra bit and drop the last word bit. Other bits (location, magnitude and word mark have been shifted 1 bit higher. The final change for the serial out selection required the inclusion of a multiplexer at the output stage and an additional control bit. Both changes are straightforward. All changes have already been implemented in the new design.

Discussion of cost and schedule concluded the review. There was discussion about the ramifications of going with an engineering run now, or a second MOSIS run. Doing a MOSIS run first, followed by an engineering run, places the FPHX chip on the critical path and absorbs most of the schedule contingency. A end of May submission would mean that chips for testing would not be available until late summer/early fall. Assuming a month of testing, submission of the engineering would then happen late 3rd quarter of CY 2009 or early 4th quarter. While delivery of engineering runs is not constrained to MOSIS submission dates and is typically faster then a MOSIS delivery. An exact delivery time is uncertain, but expected to be of order 8 weeks from submission. There is however considerable cost risk to an engineering run. A typical engineering run produces 12 wafers with a guarantee of 6 wafers. FNAL experience has been that they typically receive 10 wafers with a yield of 85% or better. For the FVTX, additional wafers would have to be ordered to provide the total number of chips required. A typical engineering run is of order $200K plus the cost of additional wafers.

The review committee wants to thank the FVTX group and FNAL design team for clear and comprehensive presentations of the testing of the FPHX chip. The groups have done an extensive amount of testing to validate the functionality of the FPHX chip. While many of the outstanding

questions about the chip performance have been answered, full testing of a detector system have just started. While many of the problems so far encountered with getting a fully functional wedge operational are not associated with the FPHX chip, however; it is necessary to test a fully functional wedge with sensor using both calibration date and source or cosmic ray data. In addition, it is important to understand operational range of the chip on the HDI. While tests have been started, it is felt that more tests need to be done and documented.

The changes so far suggested are not considered major by the design engineers, and the digital changes have already been implemented. The changes for the analog section were estimated to take 1.5 to 2 weeks. It is the feeling of the committee that an engineering run at this stage is not feasible given the status of the testing with sensor and the FVTX group should aim for June 1, 2009 MOSIS submission. If future tests of the FPHX chip with sensor and HDI continue to be promising, then an early submission of an engineering run can considered to recover some of the schedule contingency. In parallel with the MOSIS run, the FVTX group should develop a complete plan for the engineering run, that includes submission and delivery, wafer testing, thinning and dicing. The plan should also detail the expected yield at all stages, and the total number of good wafers required to achieve the required number of FPHX chips for the FVTX project. When additional testing as discussed in completed and a full production plan is available, a follow up review should be held prior to submission for an engineering run.