ROC Testing Plan

1. Get power cable tested and power one piece of the circuit at a time:
   1. Measure resistance at all power inputs
   2. Check power at each of the voltage regulators, then at each major chip
   3. Connect clock signal to ROC and check BCO/Start clock distribution works
   4. Power and program each of the FPGAs. Is lock established on each FPGA?
   5. Check power to FO chips
   6. Check FO clocks are present and being distributed
   7. Check calibration circuitry powered
2. Check basic communication chains working:
   1. Do SC clocks appear on the Hirose connectors?
   2. Can we establish FO synch with SC FO?
   3. Can we communicate with SC FPGA via FO link (send a reset, e.g.)?
   4. Can we achieve FO sync with the data FOs?
3. Power Wedges:
   1. Connect power cable and establish correct power on hirose connectors
   2. With power off, make sure wedge HDI mates with the ROC – how to protect the wedge?
   3. Connect wedge and see if current draw looks appropriate
4. Communicate with wedge:
   1. Can we send RESET/INIT commands and see appropriate current draw change?
   2. Do we see calibration pulses coming out when we start a calibration or manual pulse?
   3. Can we see sync words on hirose pads?
   4. Can we collect any data?
5. Remote FPGA programming:
   1. Attempt to remotely program every FPGA on the design (through JTAG FPGA)
   2. Test ability to program the JTAG chain once the remote programming is switched off