

4.0 Module Pin-Out

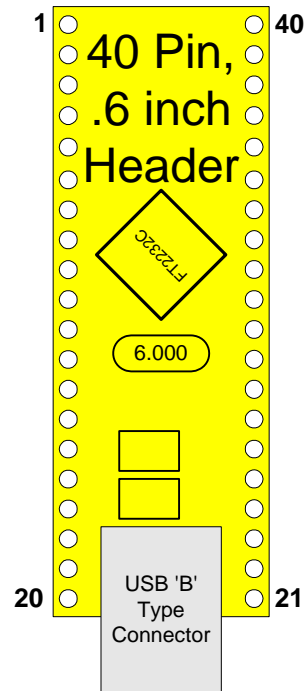


Figure 2. Pin-Out (40 Pin DIP Header)

4.1 Pin Definitions

This section describes the operation of the DLP-2232M-G pins. Common pins are defined in the first section and the I/O pins are defined by chip mode. More detailed descriptions of the operation of the I/O pins are provided in section x. (was 9)

4.2 Common Pins

The operation of the following DLP-2232M-G pins stay the same, regardless of the operating mode.

Pin#	Signal	Type	Description
27	RSTIN#	Input	Can be used by an external device to reset the FT2232D. If not required, can be left disconnected.
26	RSTOUT#	Output	Output of the internal Reset Generator. Stays high impedance for ~5ms after VCC > 3.5V and the internal clock starts up, then clamps it's output to the 3.3V output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset.
19	EXTVCC	PWR	+4.35 to +5.25 volt VCC to the device core, LDO and non-

			UART / FIFO controller interface pins. Device Analog Power Supply for the internal x8 clock multiplier.
18	VCCIOA	PWR	+3.0 to +5.25 volt VCC to the UART/FIFO Channel A interface pins. When interfacing with 3.3V external logic connect VCCIO to the 3.3V supply of the external logic, otherwise connect to VCC to drive out at 5V CMOS level.
17	VCCIOB	PWR	+3.0 volt to +5.25 volt VCC to the UART/FIFO Channel B interface pins. When interfacing with 3.3V external logic connect VCCIO to the 3.3V supply of the external logic, otherwise connect to VCC to drive out at 5V CMOS level.
20	PORTVCC	PWR	Power from USB port. Connect to EXTVCC if module is to be powered by the USB port (typical configuration). 500mA maximum current available to USB adapter and target electronics if USB device is configured for high power.
16	VCCSW	PWR	Output of the MOSFET power switch, activated after enumeration.
21	VCCUSB	PWR	Filtered +3.0 volt to +5.25 volt EXTVCC from either the host USB port or user supplied external power supply.

4.3 IO Pin Definitions by Chip Mode

The definition of the following pins vary according to the module's mode:

Pin#	Generic Pin Name	Pin Definitions by Chip Mode <i>*Note 2</i>						
		232 UART Mode	245 FIFO Mode	CPU FIFO Interface Mode	Enhanced Asynchronous and Synchronous Bit-Bang Modes	MPSSE <i>*Note 4</i>	MCU Host Bus Enumeration Mode <i>*Note 5</i>	Fast Opto-Isolated Serial Mode
40	ADBUS0	TXD	D0	D0	D0	TCK/SK	AD0	<i>*Note 3</i>
39	ADBUS1	RXD	D1	D1	D1	TDI/DU	AD1	
38	ADBUS2	RTS#	D2	D2	D2	TDO/D1	AD2	
37	ADBUS3	CTS#	D3	D3	D3	TMS/CS	AD3	
36	ADBUS4	DTR#	D4	D4	D4	GPIOL0	AD4	
35	ADBUS5	DSR#	D5	D5	D5	GPIOL1	AD5	
34	ADBUS6	DCD#	D6	D6	D6	GPIOL2	AD6	
33	ADBUS7	RI#	D7	D7	D7	GPIOL3	AD7	
32	ACBUS0	TXDEN	RXF#	CS#	WR# <i>*Note 6</i>	GPIOH0	I/O0	
31	ACBUS1	SLEEP#	TXE#	A0	RD# <i>*Note 6</i>	GPIOH1	I/O1	
30	ACBUS2	RXLED#	RD#	RD#	WR# <i>*Note 7</i>	GPIOH2	IORDY#	
29	ACBUS3	TXLED#	WR	WR#	RD# <i>*Note 7</i>	GPIOH3	OSC	
28	SI/WUA	???	SI/WUA	SI/WUA		SI/WUA		

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13	BDBUS0	TXD	D0	D0	D0		AD8	FSDI
12	BDBUS1	RXD	D1	D1	D1		AD9	FSCLK
11	BDBUS2	RTS#	D2	D2	D2		AD10	FSDO
10	BDBUS3	CTS#	D3	D3	D3		AD11	FSCTS
9	BDBUS4	DTR#	D4	D4	D4		AD12	<i>*Note 3</i>
8	BDBUS5	DSR#	D5	D5	D5		AD13	
7	BDBUS6	DCD#	D6	D6	D6		AD14	
6	BDBUS7	RI#	D7	D7	D7		AD15	
5	BCBUS0	TXDEN	RXF#	CS#	WR# <i>*Note 8</i>		CS#	
4	BCBUS1	SLEEP#	TXE#	A0	RD# <i>*Note 8</i>		ALE	
3	BCBUS2	RXLED#	RD#	RD#	WR# <i>*Note 7</i>		RD#	
2	BCBUS3	TXLED#	WR	WR#	RD# <i>*Note 7</i>		WR#	
1	SI/WUB	???	SI/WUB	SI/WUB				

**Note 2* : 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using driver commands.

**Note 3* : Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

**Note 4* : MPSSE is Channel A only.

**Note 5* : MCU Host Bus Emulation requires both Channels.

**Note 6* : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

**Note 7* : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

**Note 8* : The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.