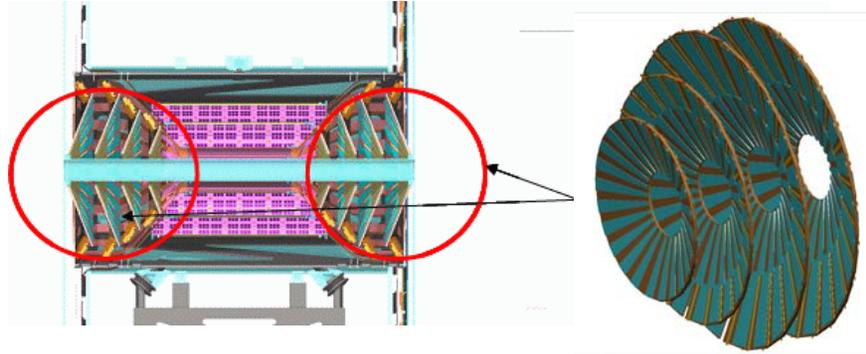


FVTX Proposal Update



- Matching MuTr and Silicon tracks in Central AuAu (Melynda, Xiaorong)
- Rejection/Acceptance of Background/Signal versus momentum (Anuj)
- Updated J/ψ , ψ' plots (Xiaorong)
- Additional studies of resolution with “straight” planes (Hubert)
- Cable routing and space (Walt, Jan)
- Ongoing work in the lab (Gerd, Anuj, Sergey, Melynda, Pat)
- Cost and Schedule updates ongoing (Dave, Melynda starting)
- Proposal updates (Mike)

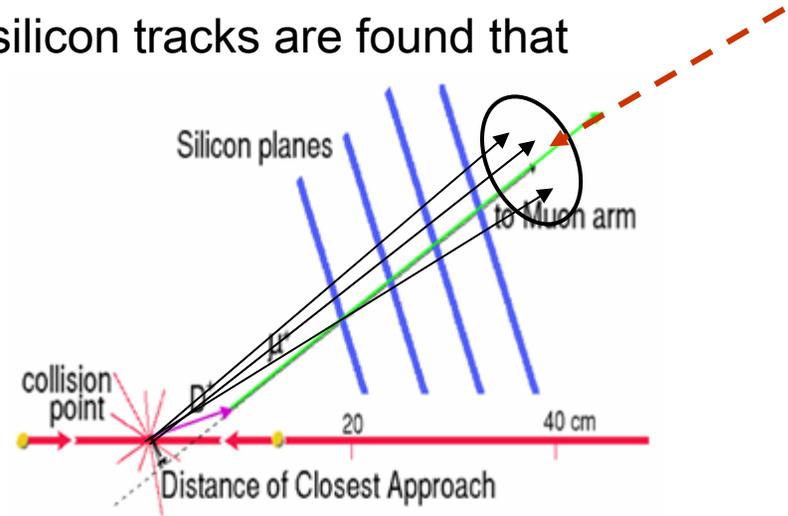
Matching MuTr and Silicon tracks in Central AuAu

Addressing Review Comment:

1. It must be verified that muon tracks can be connected to tracks in the FVTX in Au+Au collisions.

Matching MuTr and Silicon tracks in Central AuAu

Issue: in Central AuAu events, approximately 3 silicon tracks are found that approximately match each MuTr track



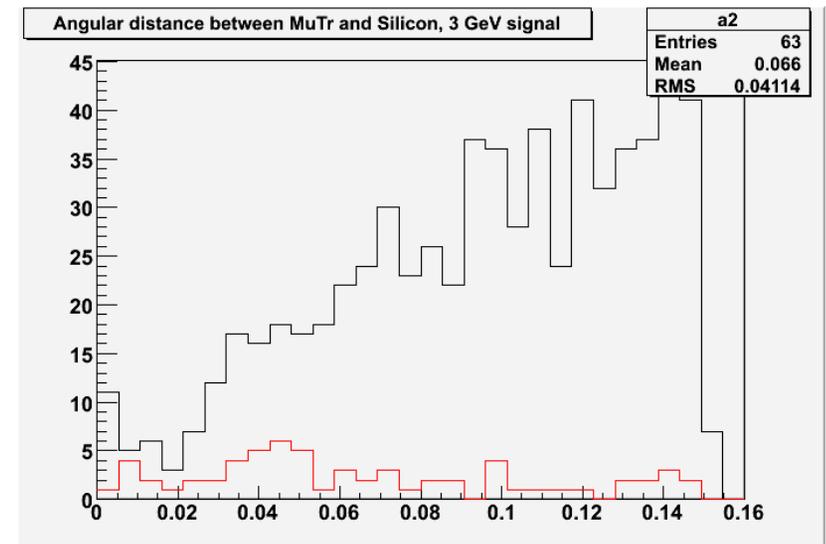
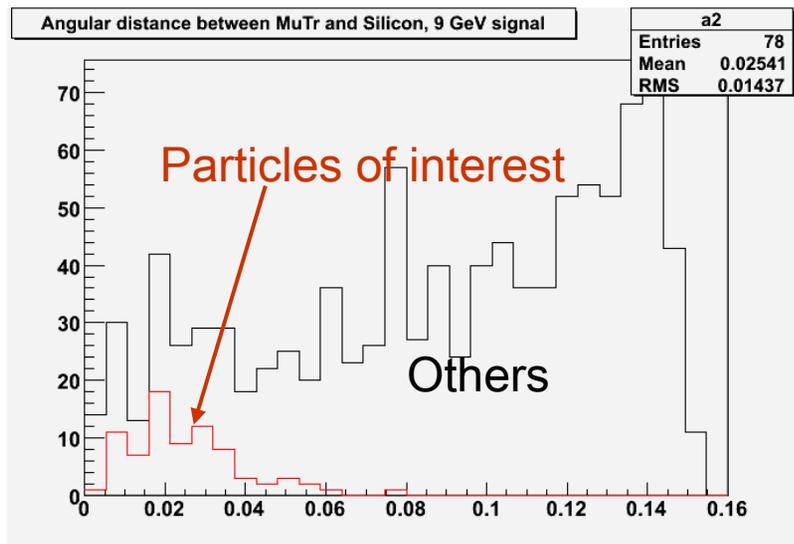
Solutions:

- As shown last update, all but one of these can on average be rejected just by removing all silicon tracks with $\chi^2 > \chi^2_{\text{Max}}$
- Look at additional rejection that can be obtained if you use a Kalman-Filter fit to MuTr+Silicon hits and choose best χ^2
- **Caveats on study to-date:**
 - Full digitization of hits is not completed so PISA hits have been used (but remember multiple scattering is dominant contributor to resolution in many cases)
 - Perfect pattern recognition in the silicon (all hits which go with a particular MC track are grouped together)

Matching MuTr and Silicon tracks in Central AuAu

Study:

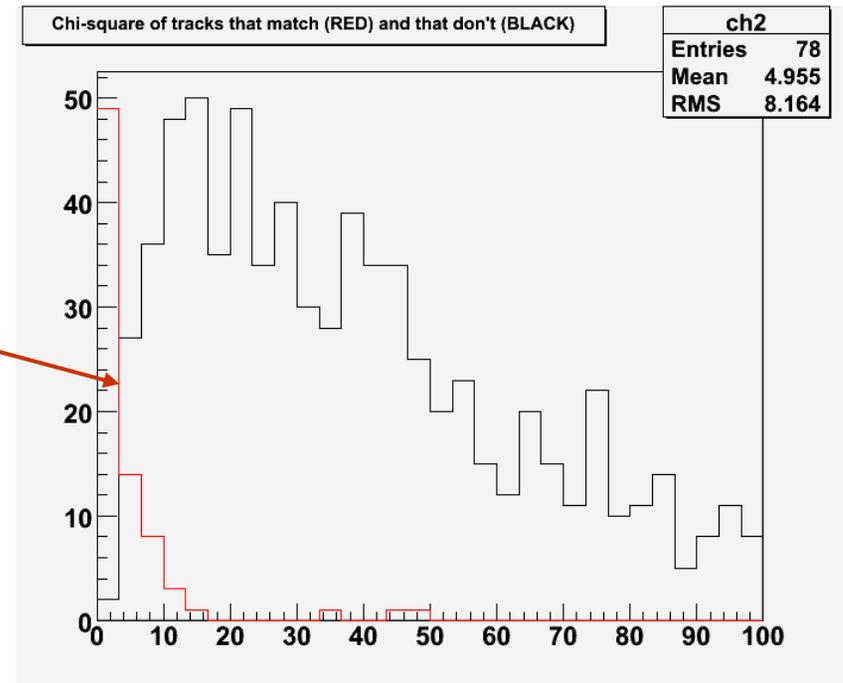
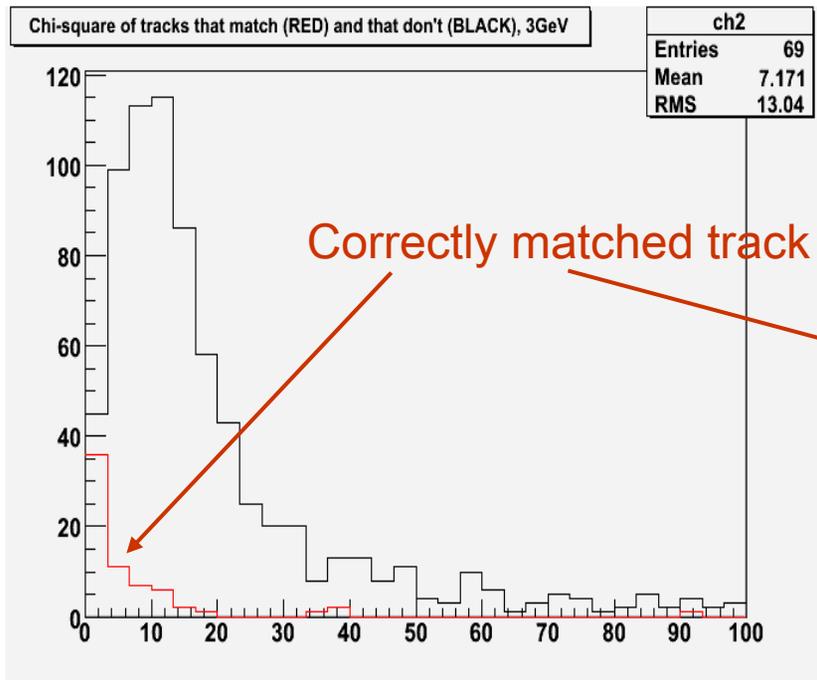
- Mix Central AuAu events with single muons
- For mixed track:
 - Find MuTr track which has most MC contributor hits (reconstructed track)
 - Find all silicon stubs that are within a 2-d angular window of this track
 - Fit each set of potential silicon hits with the MuTr track and store fit results
 - Look at distributions for tracks that are properly matched and those that are not
 - Attempt to select best match, just using χ^2



Matching MuTr and Silicon tracks in Central AuAu

Rejection:

- Pick track with best χ^2 : 93%, 83%, 75% of the time the correct match is made for 9 GeV, 6 GeV, 3 GeV particles



Matching MuTr and Silicon tracks in Central AuAu

To Do:

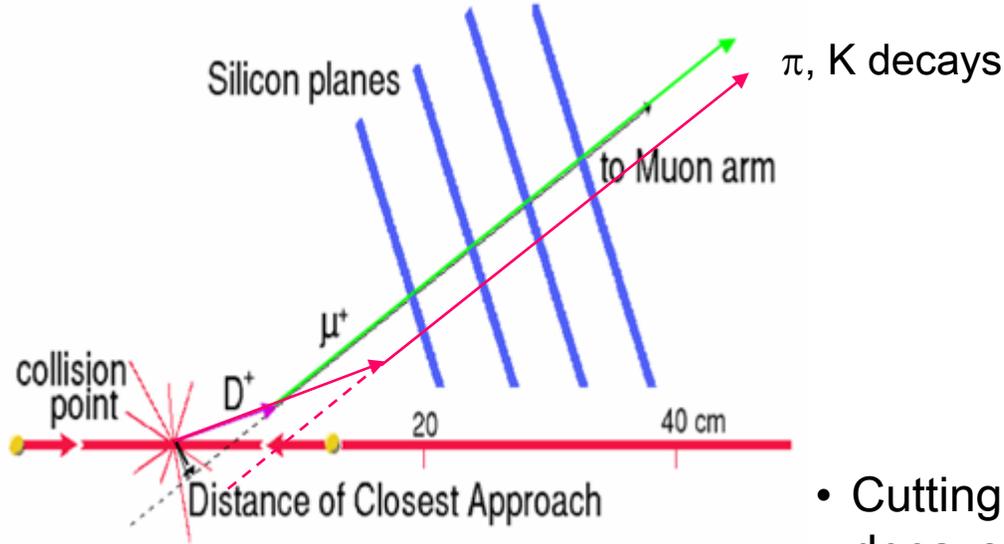
- Efficiency looks good already, but would like to complete studies of:
- Finish digitization and recalculate efficiency
- Mix realistic spectrum of B, D decays and check efficiency (*think* this should only make things better, but...)
- Look at possibility of also rejecting hadrons which interact somewhere along the path or decay somewhere before reaching the MuID

FVTX Contributions—Reduction of Decay Background

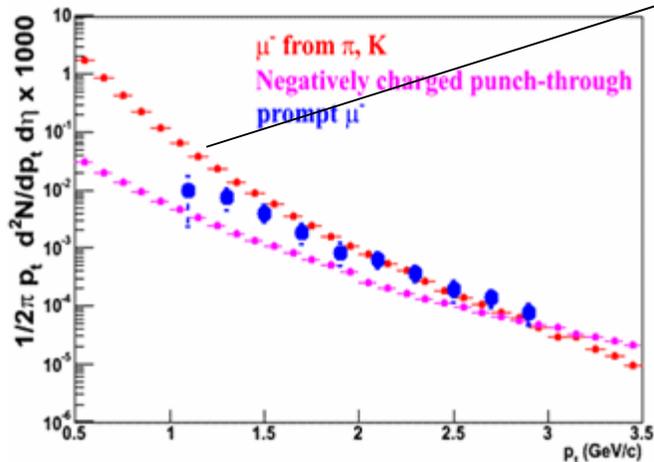
Addressing Review Comment (?):

4. The separation of b and c decays based on decay length with reasonable RHIC II luminosity should be shown

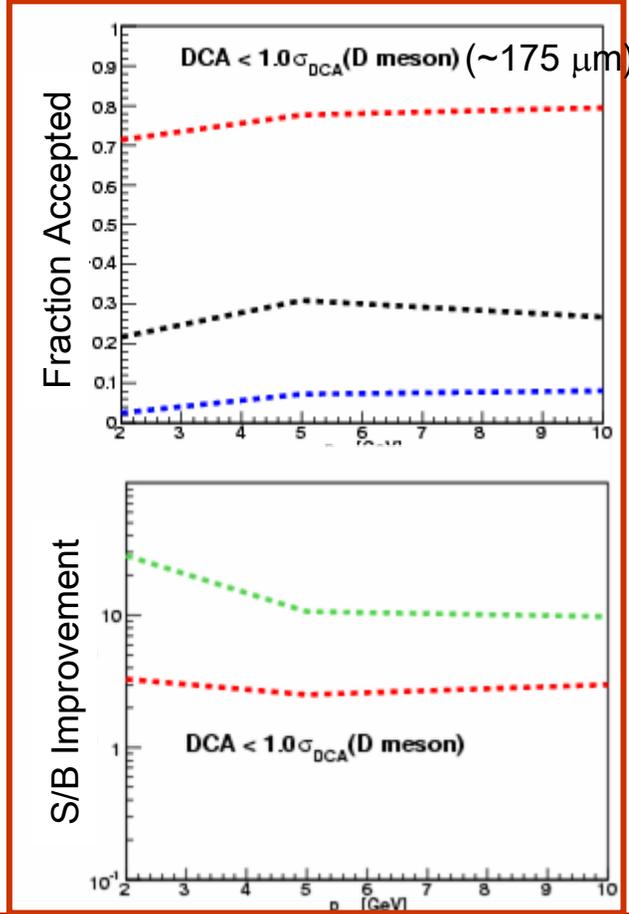
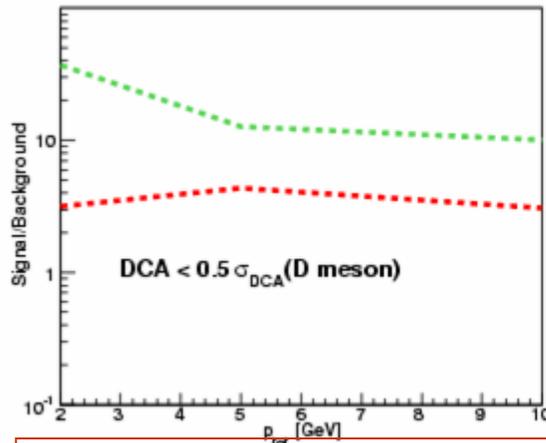
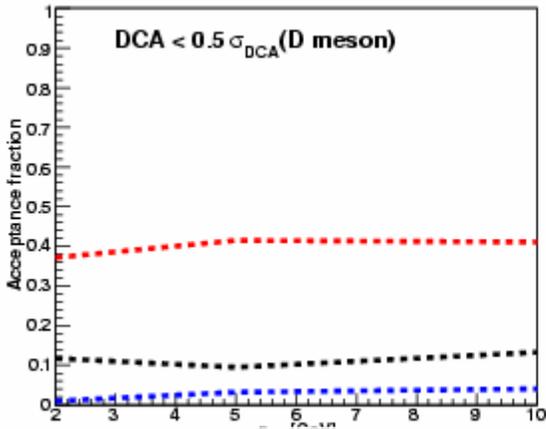
FVTX Contributions—Reduction of Decay Background



- Cutting on $DCA < DCA_{max}$ allows long-lived π, K decays to be separated from heavy quark decays AND cleaner sample of π, K at forward rapidity
- Especially necessary to access low p_T spectra



FVTX Contributions—Reduction of Decay Background



Accepted D muons

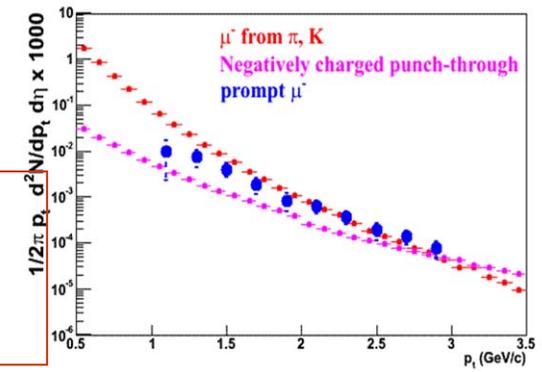
Accepted π muons

Accepted K muons

Signal:Back improvement for:

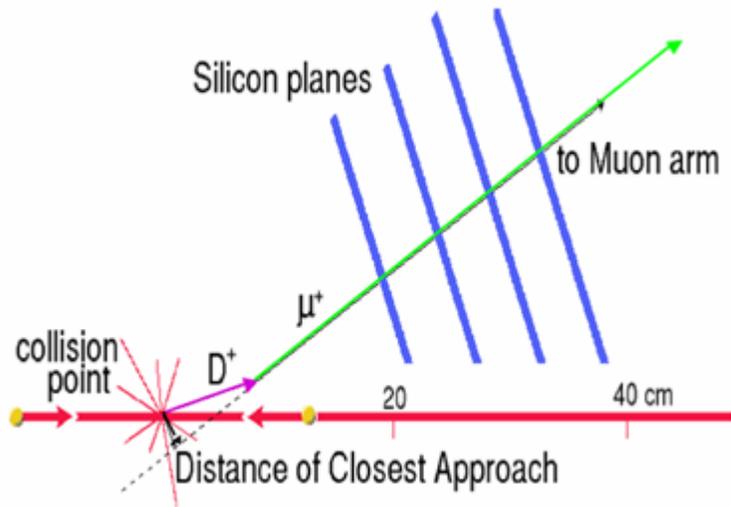
D:K

D: π

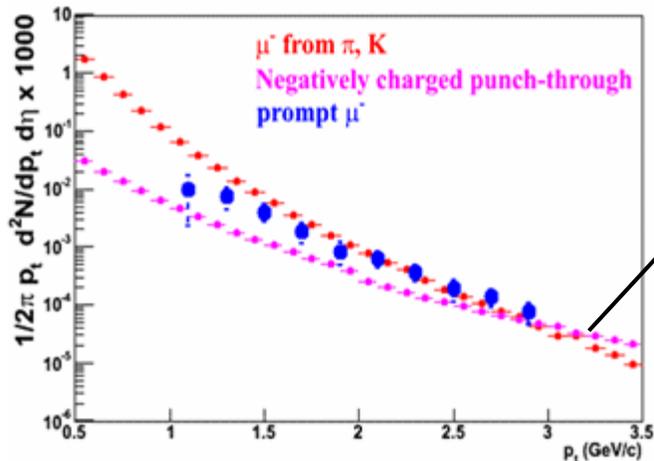


Background will be brought below signal level at all momenta, plus more rejection may be possible with more sophisticated cuts

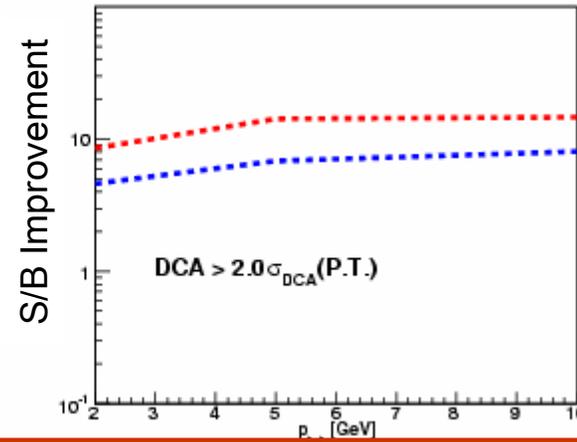
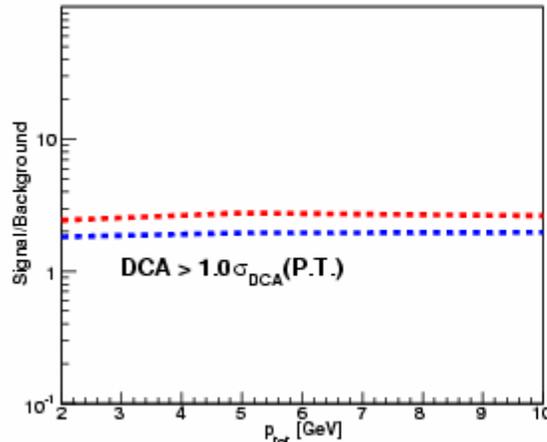
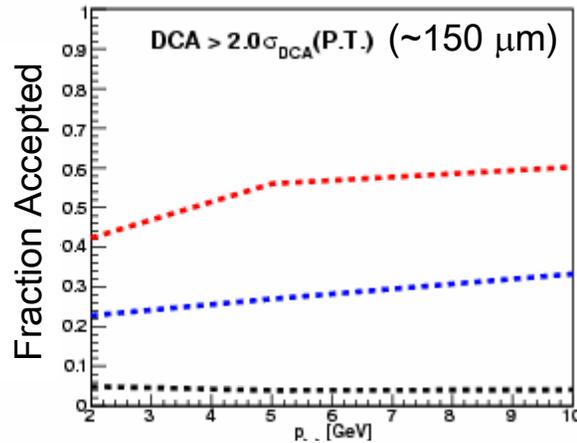
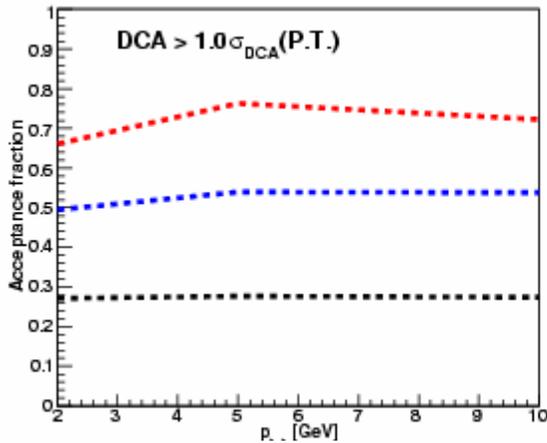
FVTX Contributions—Reduction of Punch-Throughs



- Cutting on $DCA > DCA_{\min}$ allows π, K punch-throughs (prompt) to be separated from open heavy flavor decays
- Especially necessary to access high p_T spectra



FVTX Contributions—Reduction of Punch-Throughs



Accepted B muons

Accepted D muons

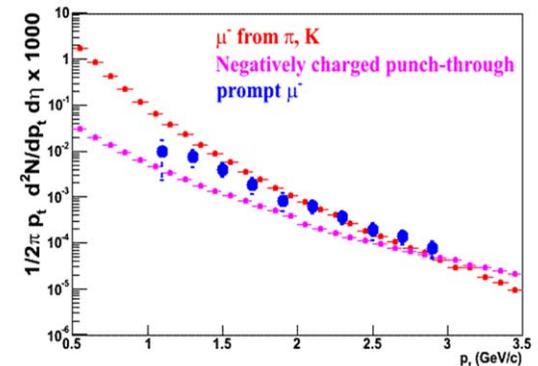
Accepted punch-through hadrons

Signal:Back improvement for:

B:punch-through

D:punch-through

Signal:background even for μ^+ should be made $\gg 1$

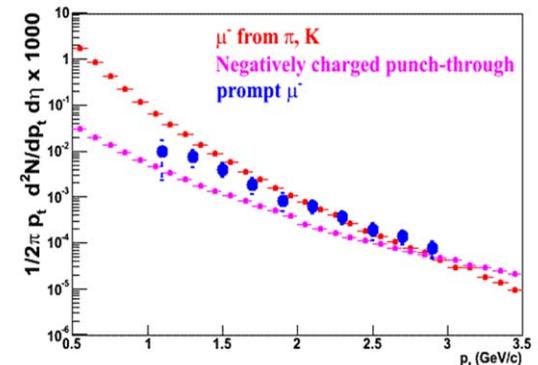


FVTX Contributions—Reduction of Hadrons

To Do:

Rejection already looks good, but would like to complete:

- Make combined performance plot with both DCA cuts applied to realistic spectra
- Make physics sensitivity plots with above
- Add in primary vertex resolution (in progress)



J/ψ , ψ' Measurement Improvement with FVTX

Addressing Review Comment :

3. The statistical significance of the ψ' in Au+Au collisions with a reasonable RHIC II luminosity should be shown.

J/ ψ , ψ' Measurement Improvement with FVTX

- AuAu Central (left)
- AuAu MinBias (right)

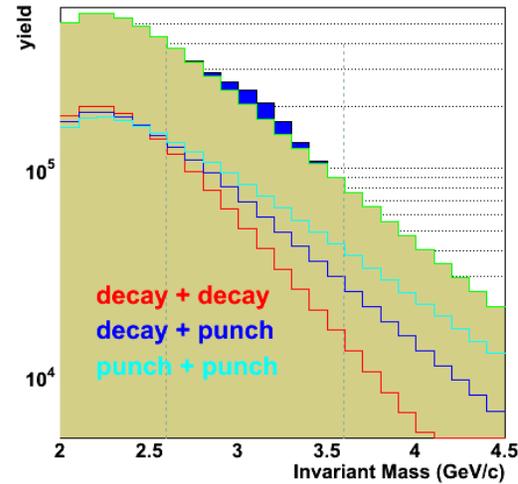
without and with FVTX :

- mass resolution improvement
- background rejection

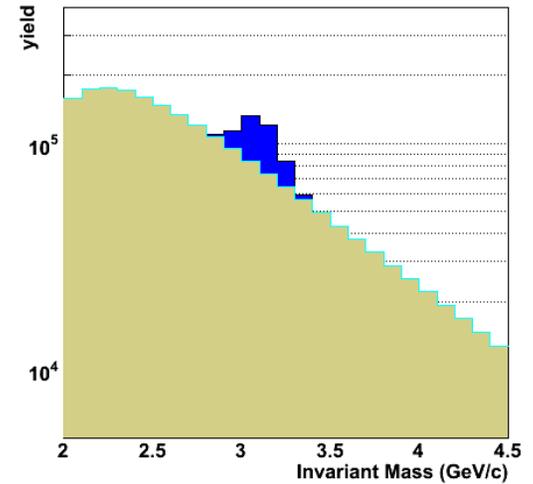
- Baseline S:B from real data

• Note: similar plots can be made for upsilons

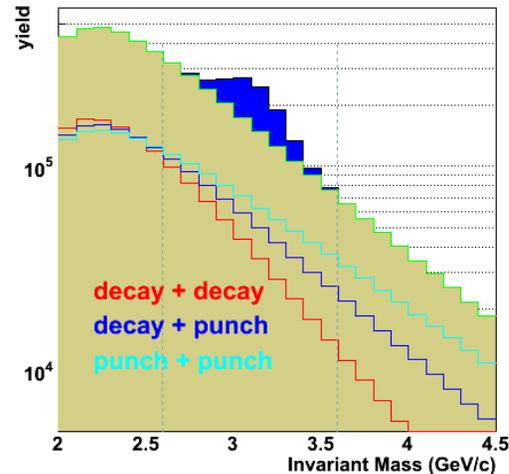
Dimuon invariant mass distribution



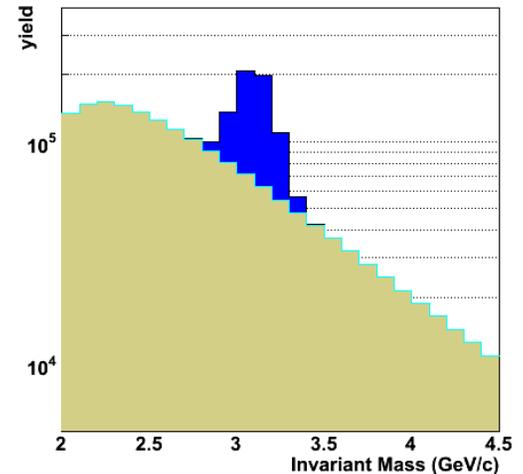
Dimuon invariant mass distribution



Dimuon invariant mass distribution



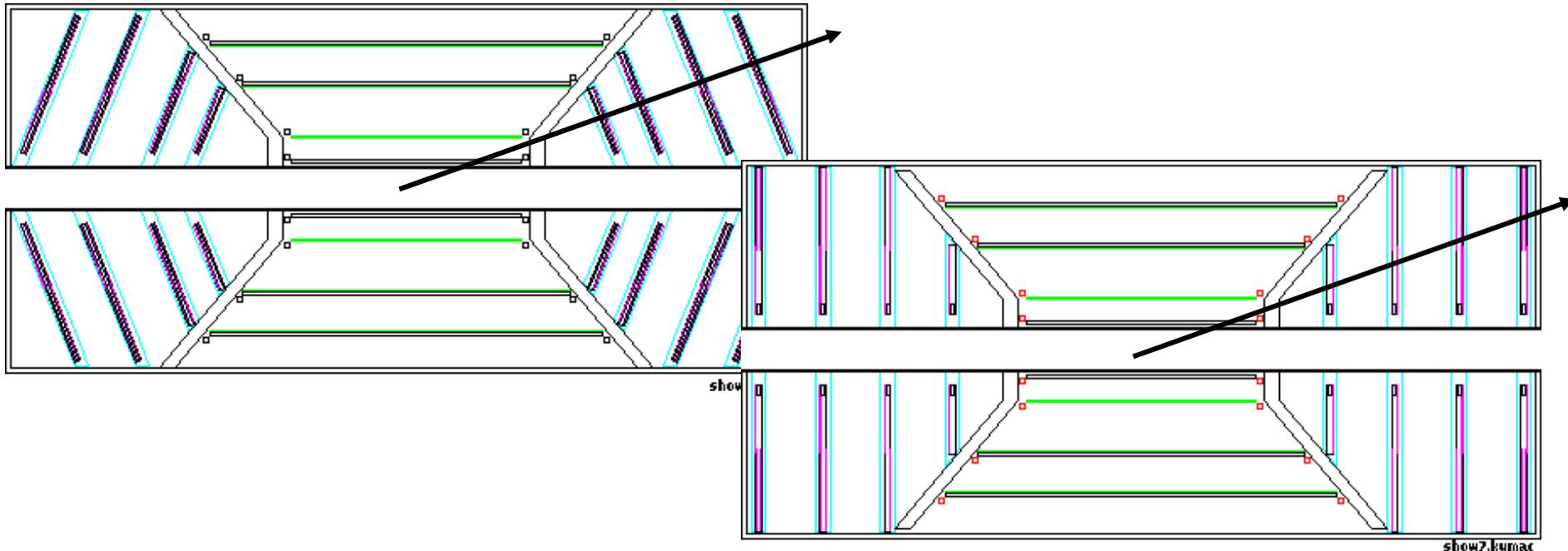
Dimuon invariant mass distribution



Silicon Orientation, Strip Width, and Thresholds

Hubert is actively looking at the performance of the system with:

- “straight” versus “umbrella” orientation of the layers (mechanically simpler, may require fewer channels...)
- Resolutions obtained from full cluster reconstruction rather than just centroid strip
- How resolutions change with different threshold cuts
- How resolutions change with different strip widths, but using clustering



Silicon Orientation, Strip Width, and Thresholds

Increasing the threshold for a given strip width gives smaller cluster sizes but resolution doesn't change too much as long size ≥ 2 :

- Note previous studies all used 1-strip resolution, $50\mu\text{m} \rightarrow 14.4\mu\text{m}$ resolution

	Threshold					
	25	34	50	75	125	
#clusters size=1	437	639	1132	2876	13918	
mean cluster size	2.9	2.8	2.6	2.3	1.8	
n3/n2	1.6	1.4	1.0	0.52	.25	
Resolution	8.6	9.5	9.5	9.6	8.2	

Silicon Orientation, Strip Width, and Thresholds

You may want to investigate larger strip spacing if resolution has improved (but unneeded) because of multi-hit clusters

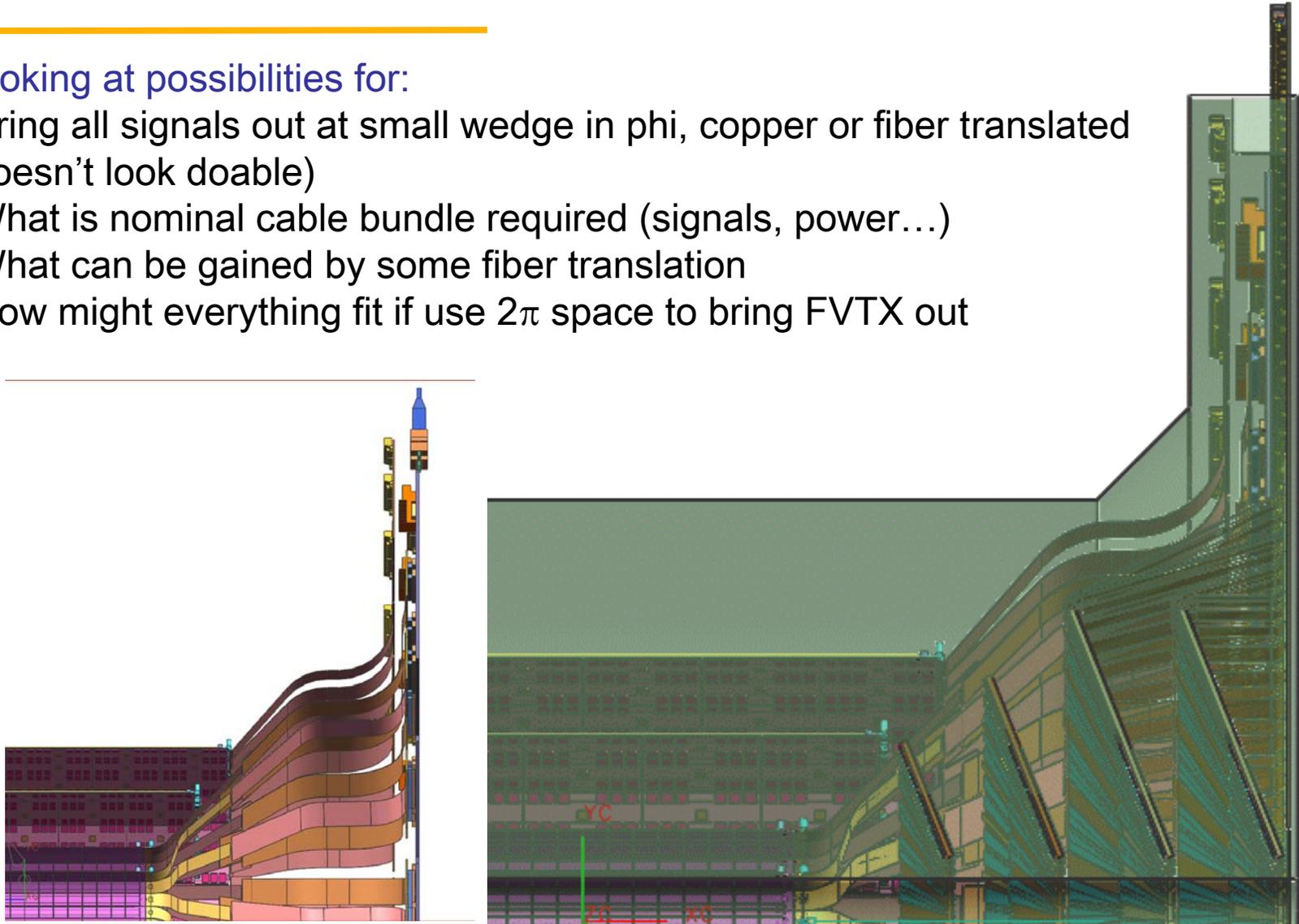
- Resolution changes as expected, ~proportional to strip width
- Note previous studies all used 1-strip resolution, $50\mu\text{m} \rightarrow 14.4\mu\text{m}$ resolution

	Strip width				
	50	75	100	200	
Threshold	25	34	50	75	
#clusters size=1	437	2757	7347	22743	
mean cluster size	2.9	2.3	1.9	1.3	
Resolution	8.6	15.3	21.4	36.3	
strip/sqrt(12)	14.4	21.6	28.9	57.7	

Space Issues

Looking at possibilities for:

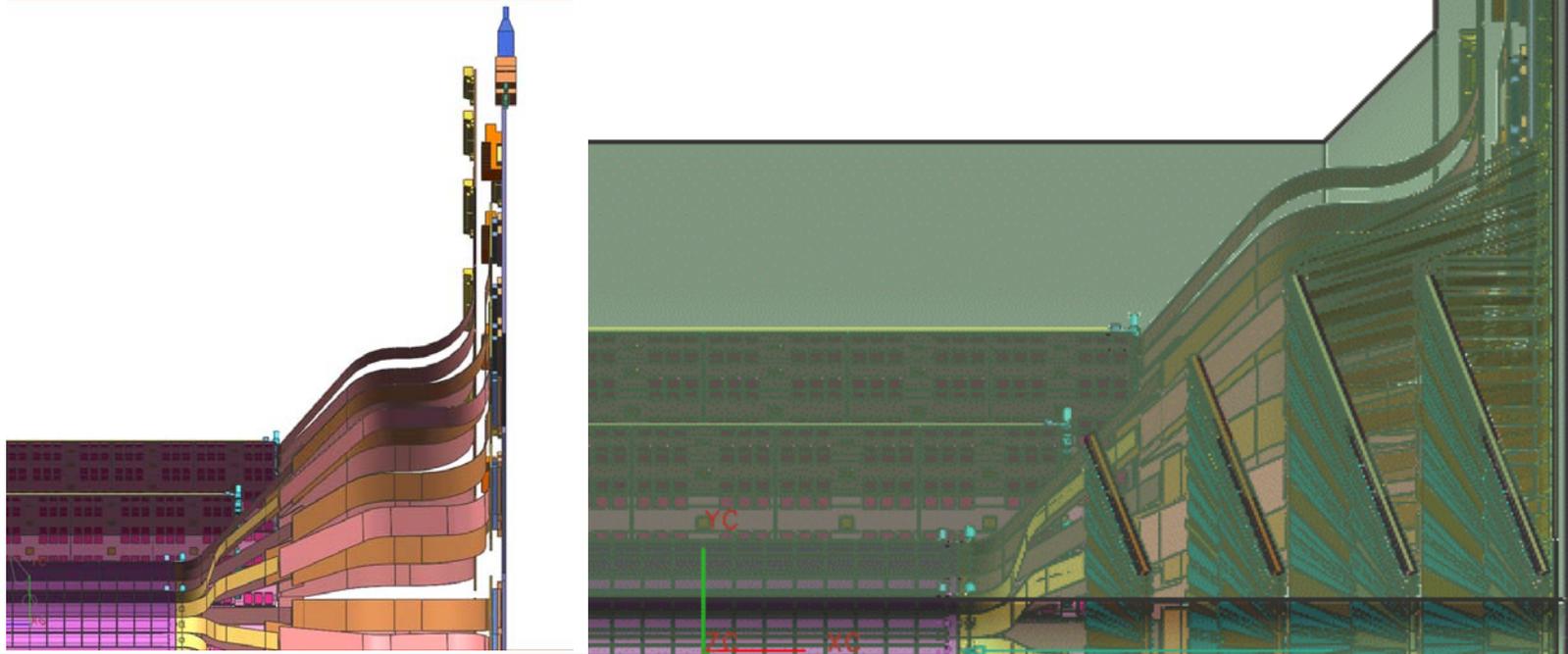
- Bring all signals out at small wedge in phi, copper or fiber translated (doesn't look doable)
- What is nominal cable bundle required (signals, power...)
- What can be gained by some fiber translation
- How might everything fit if use 2π space to bring FVTX out



Space Issues

Status:

- Jan has determined how various connectors that could carry all our (FVTX) copper or fiber might fit – everything is tight
- Vince, Atsushi, Raphael transferred much info to Jan/Walt on barrel constraints – likely more issues with fitting in the z constraints



Space Issues

Make conservative estimate of number of (copper) lines required for FVTX (all PAIRS)

- See below for counts
- $(2 \text{ ladders}) * (4 \text{ layers}) * (48 \text{ wedges/layer}) = 384$ connectors per arm
- Fiber option may not be much better because fiber count is reduced but connectors tend to be bigger, require additional chips not needed for copper, and still need to bring in some copper. Heat load.



Number of Chips	Number of Readout Lines/Chip	Data Lines (pairs)	Clock (from Chips)	Downloaded lines (pairs)	Calibration Lines (Pulser, Control)	Power + Ground (Vdd, Vda, HV) (pairs)	Cooling Lines	Copper Pairs needed	Copper Data Lines Needed	Total (Data + Power +)
6	4	24	6	6	2	3		41	82	88
5	4	20	5	6	2	3		33	72	78

Lab Progress

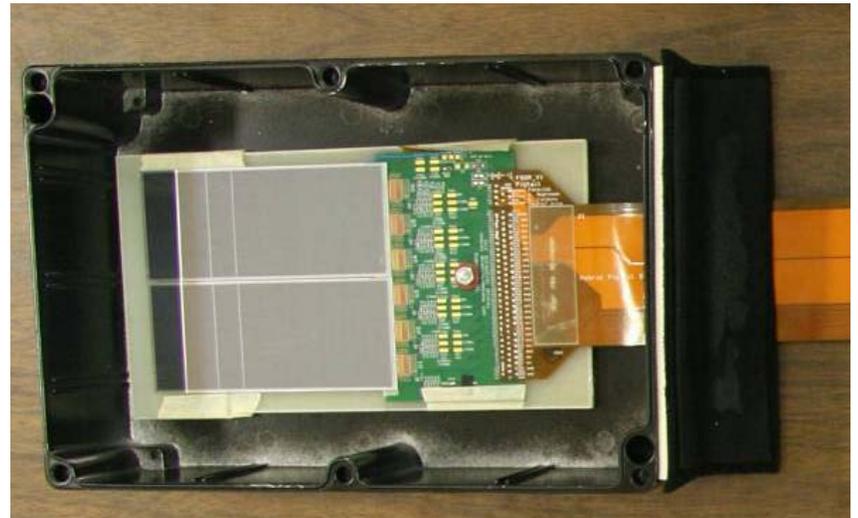
Working with single-chip FSSR, 6-chip FSSR

- Both up and working at LANL
- Much learned about details of chip operation and interface issues in the process
- Expect to move to noise measurements, driver capabilities, pushing the readout occupancy of the chip... shortly

Columbia getting lab up and running

FPGA work:

- Much work by Sergey especially on writing and testing various memory modules which can store/manage “fake” FSSR data. Mostly WORKING
- Deserializer also written and in process of testing (Anuj)
- Plan to use this code in conjunction with Fermilab chips to exercise system and see if any issues that would cause difficulties in PHENIX



Main Idea for Test Stand

- Use Xilinx Spartan-3 Starter Kit Board with XC3S200 FPGA (200K gates)
- Create PC parallel port interface
 - 3 control lines output for handshake with FPGA
 - 4 signal lines input
- Use 50 MHz internal clock for FPGA
- Mimic output from the chip on FPGA level

First Results

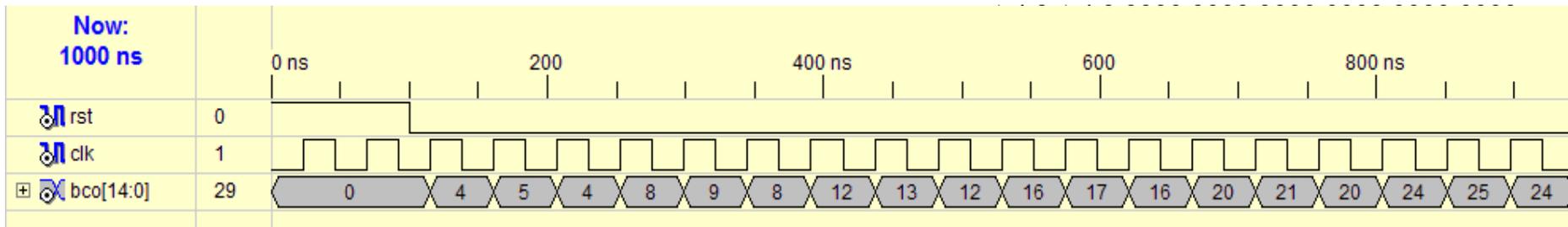
Up to 8 hits per BCO

- Send to the input 0,1,2,3 hits for one clock counter (BCO)
- Make BCOs NOT all time-ordered
- Fill BCO into memory locations
- Dump memory
- Remaining issues:
 - A few random numbers show up in non-hit locations
- Other than that memory manager works as designed

Store data words in location per BCO

```

1a80 1a80 0000 0000 0000 0000 0000 0000
1a81 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
1a84 1a84 0004 0000 0000 0000 0000 0000
1a85 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
1a88 1a88 0000 0000 0000 0000 0000 0000
1a89 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
1a8c 1a8c 0000 0000 0000 0000 0000 0000
1a8d 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
1a90 1a90 0000 0000 0000 0000 0000 0000
1a91 0000 0000 0000 0000 0000 0000 0000
.....
1ab5 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0000
    
```



Other Review Comments

5. The sensors should use standard thickness silicon. – Accepted. All work assumes 300 μm sensors now
6. A lead electronic engineer who will be available to the project for its duration should be identified. – Eric Mannel has agreed to be FVTX engineer as well as VTX engineer

Other Progresses

Cost and Schedule

- Dave (myself starting) continues to incorporate new information into cost and schedule—new quotes, added lab overheads, etc.

Proposal

- Proposal continues to be updated: some more in the physics section, New Lvl-1 section from Iowa, will incorporate all new simulations shown today
- Expect to release mid-February to reviewers, as per Ed's suggestion

Collaborators

- List is same, but will try to get commitments or not from “interested parties” list