OB HIC Production Test & QA

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Outline

OUTLINE

① Introduction

② Test Setups

③ Software

④ Progress Monitoring and First Results

⑤ New Tests

Introduction

Goals of HIC Characterisation & QA:

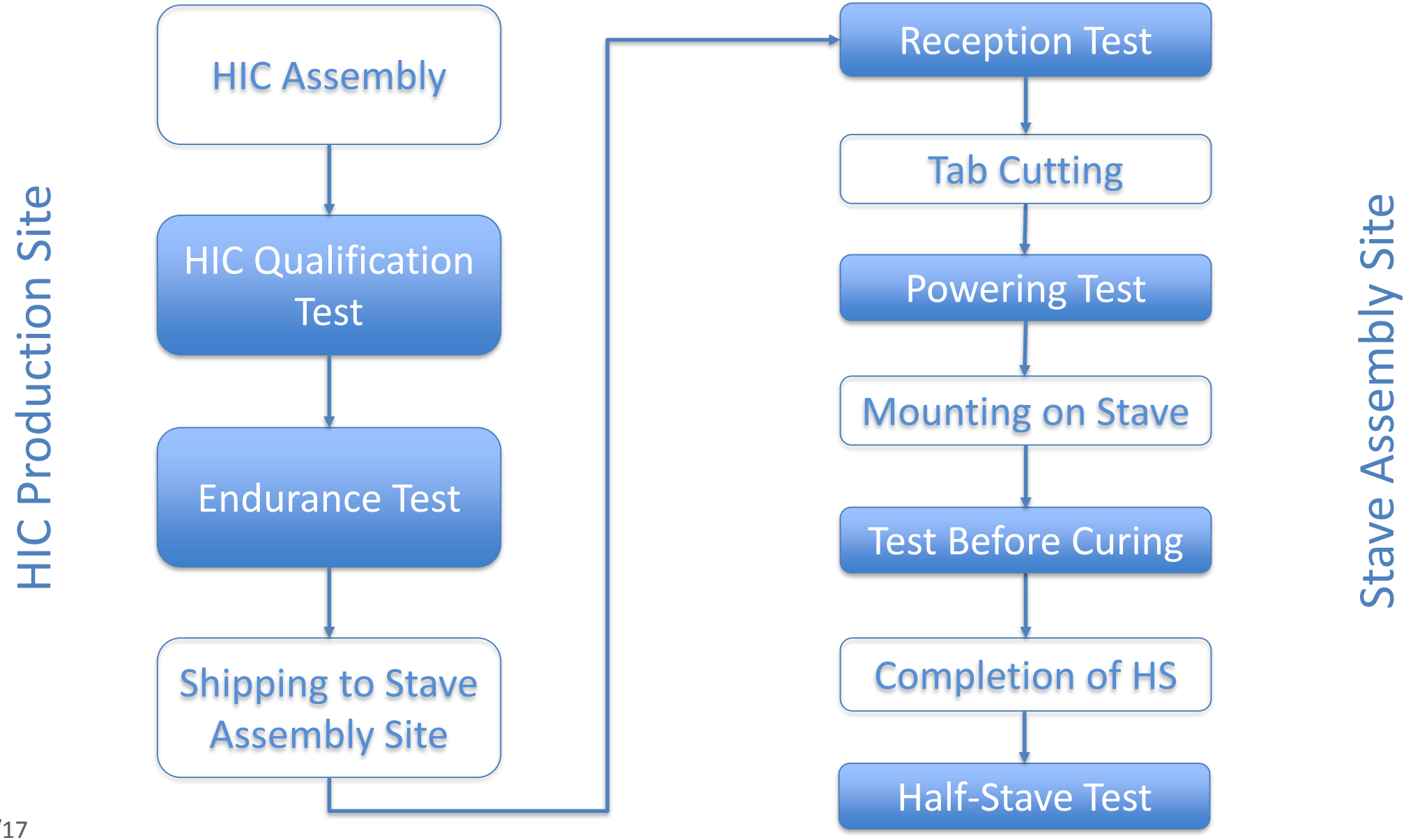
- Guarantee that only high-quality HICs are used in the detector
- Guarantee that these HICs can be operated also under real-life conditions
- Guarantee as far as possible that these HICs last for a long period of time
- Characterise the HICs

HIC Characterisation & QA is essential to guarantee the high quality of the finished detector!

-> Measurement program consisting of measurements in all steps of the assembly procedure

Different test stages involve different detector structures (single or multiple HICs, half-staves) and different measurement programs, but goal was to have coherent approach with identical user interface for all tests

Overview


HIC Production Site
HIC Assembly
HIC Qualification Test
Endurance Test
Shipping to Stave Assembly Site
Stave Assembly Site
Reception Test
Tab Cutting
Powering Test
Mounting on Stave
Test Before Curing
Completion of HS
Half-Stave Test

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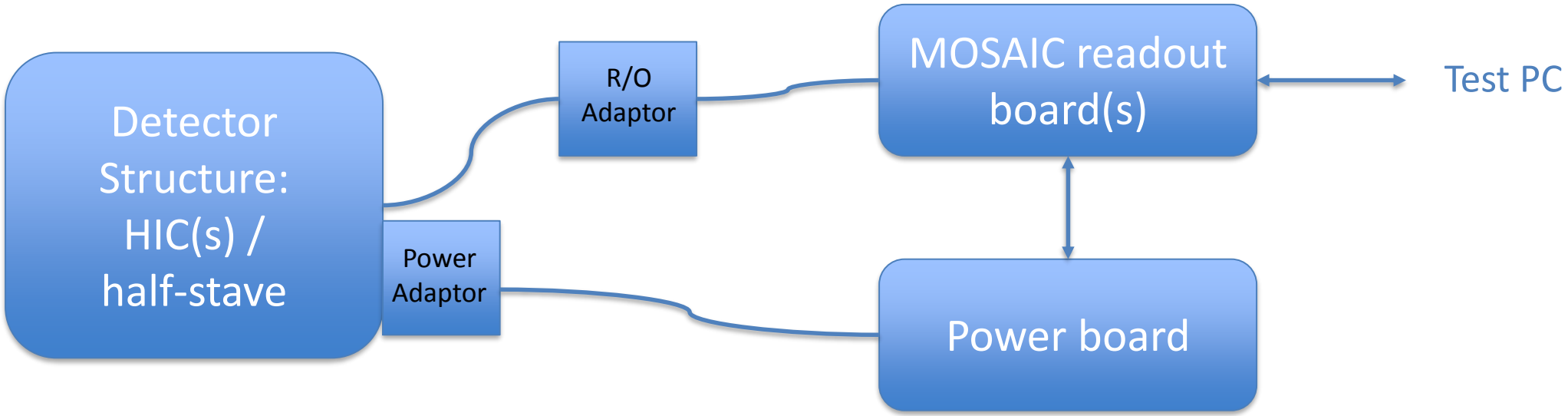
Test Setup

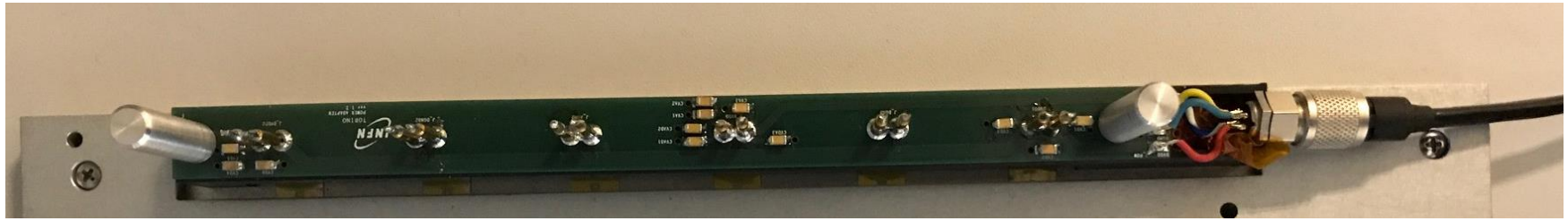
General layout of test setup:

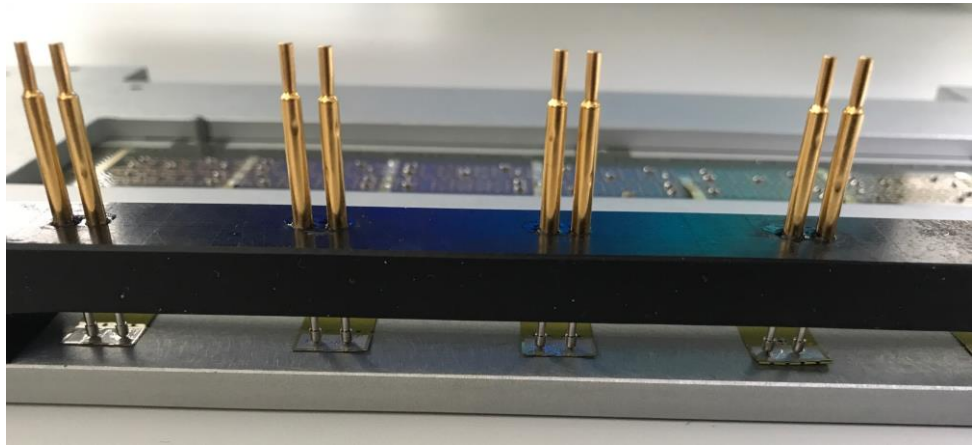
- Configuration and readout done with MOSAIC board; dedicated R/O adaptors adapt to specific detector part
- Powering done with power board
- Power adaptor allows reversible connection to cross-cables

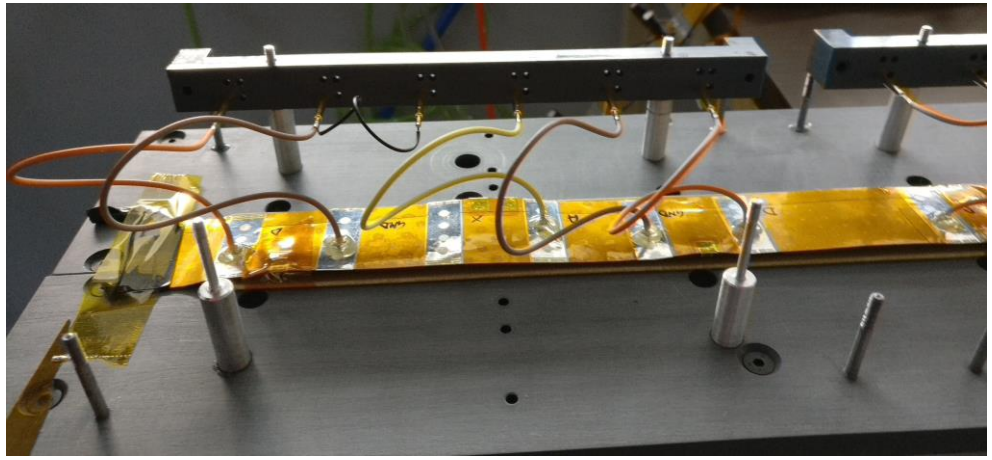


Power Adaptors

- Spring-loaded power adaptors to connect supply voltages and bias to cross-cables
- Power adaptor mounted on support plate after assembly, removed only for transport
- Slightly different versions for HICs and half-staves (bottom right)





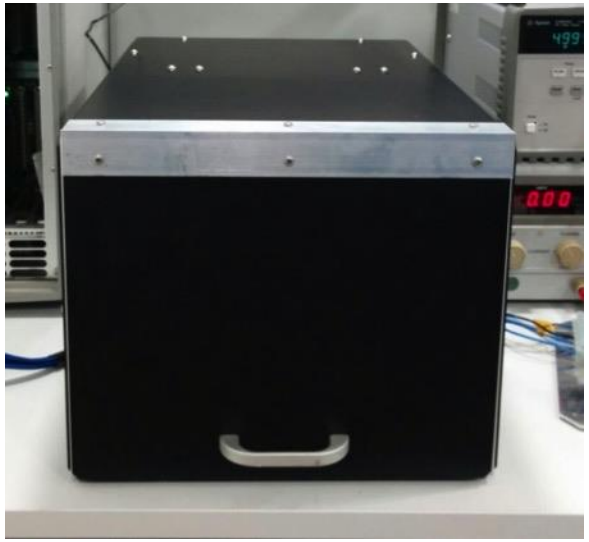


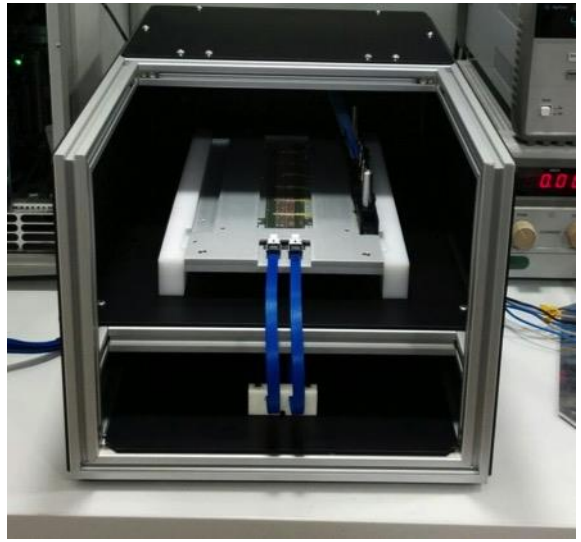
Readout Adaptors

- Several different readout adaptors according (IB HIC, OB HIC, OB Half-stave) to map ctrl and data lines from FireFly cable (HIC side) to EyeSpeed cable (MOSAIC side)
- Special case endurance test: Separate data lines and control lines on MOSAIC side to accommodate 5 OB HICs

Test Boxes

- Test boxes provide ventilation and shielding from light
- R/O adaptors and cabling integrated into box
- Two different types of boxes:
  single HIC and endurance test (10 HICs)
- Single HIC Test Boxes distributed
- First three endurance test boxes finished
- Last two this week / beginning January



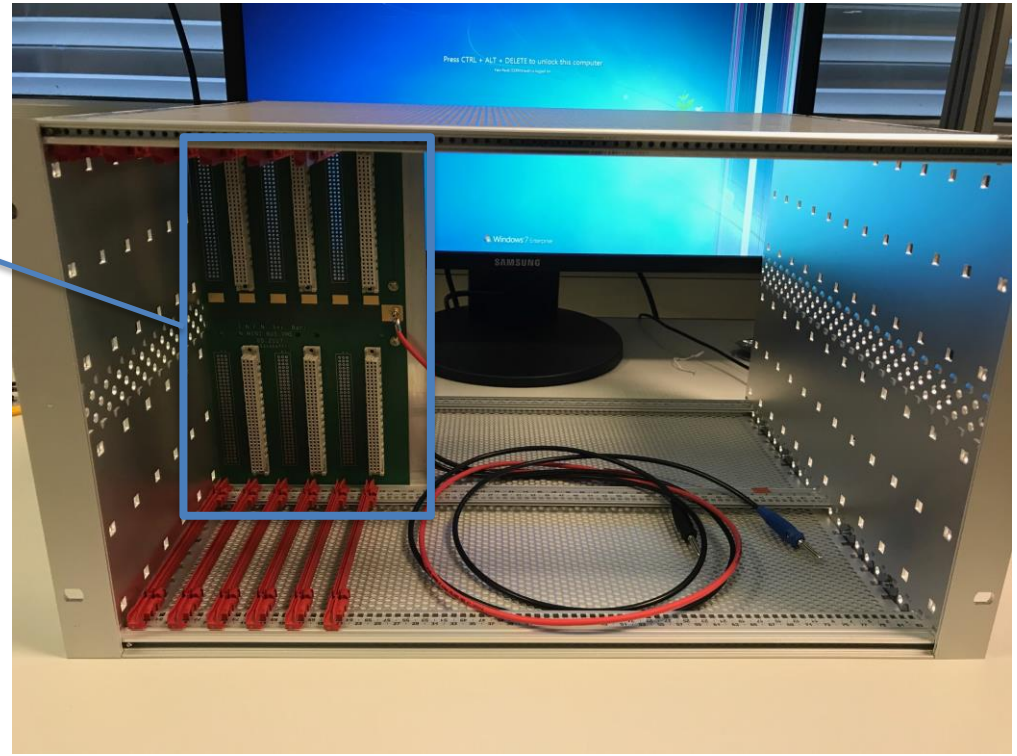


Crates

Low-cost, custom crates to house MOSAIC and power boards

- Designed for up to 3 MOSAIC boards
- Distributed 1 crate per HIC site, 1 per stave site

VME-type back plane
(power only)
for MOSAIC boards



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Test Software

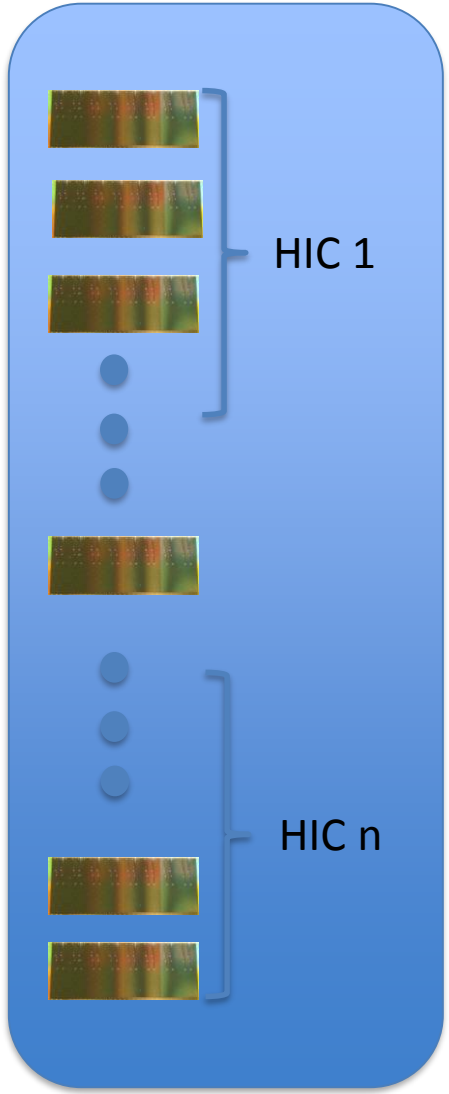
Requirements:

- To be used for different setups
- Perform large variety of different scans
- Robust also for large amounts of data
- User friendly GUI

Software :

- Decouple setup definition from scans
- Hide particular properties of the scan from the GUI
- Low-level implementation based on software library used in Alpide characterisation

Setup Definition



Chip vector:

- Based on TAlpide object from chip characterisation campaign

- Most scans act on chip objects
- HIC object used for
  - Tests where the natural granularity is the HIC (Powering tests, I-V-curve)
  - Database “granularity”

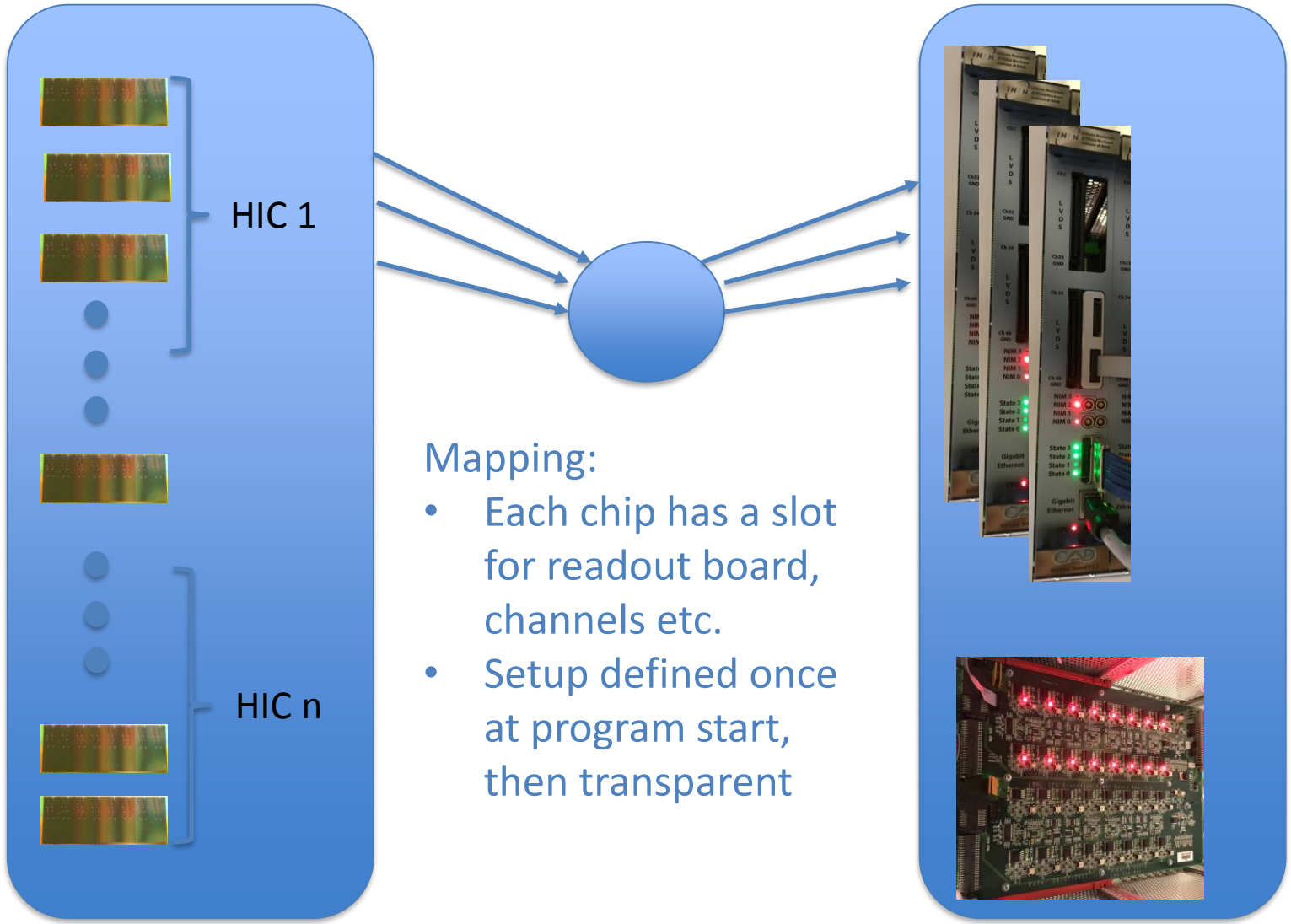
Setup Definition

Readout Board vector:

- Vector of objects that control the chip and receive data
  - (DAQ board)
  - MOSAIC
  - Readout unit

- Optional: add power board
  (controlled through the readout board)

Setup Definition

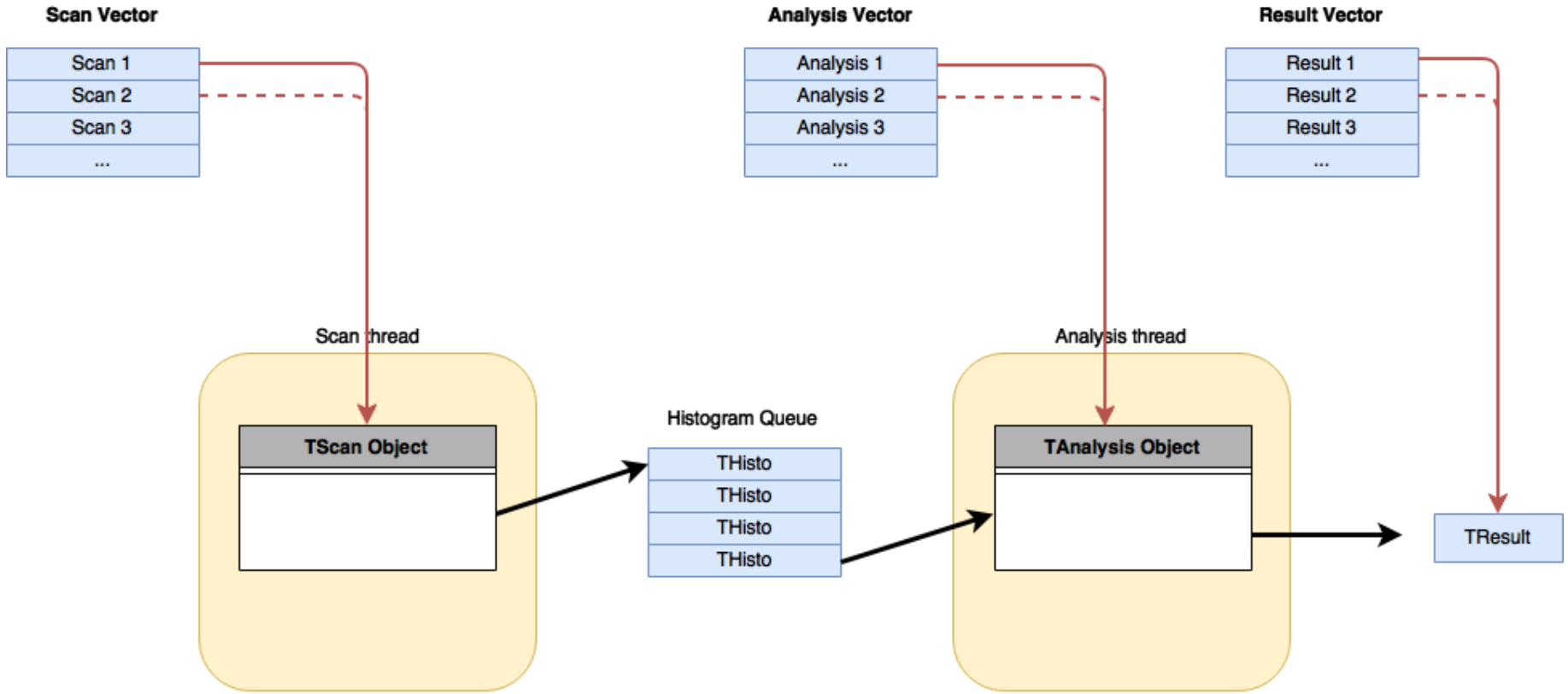


Mapping:

- Each chip has a slot for readout board, channels etc.
- Setup defined once at program start, then transparent

Scan Class

- All scans derived from generic scan class; same for analyses and scan results
- On top level (GUI): Measurement program is translated into three vectors of these generic classes (scans, analyses and results)
- Always one scan and its analysis are performed in two parallel threads (mainly for scalability)



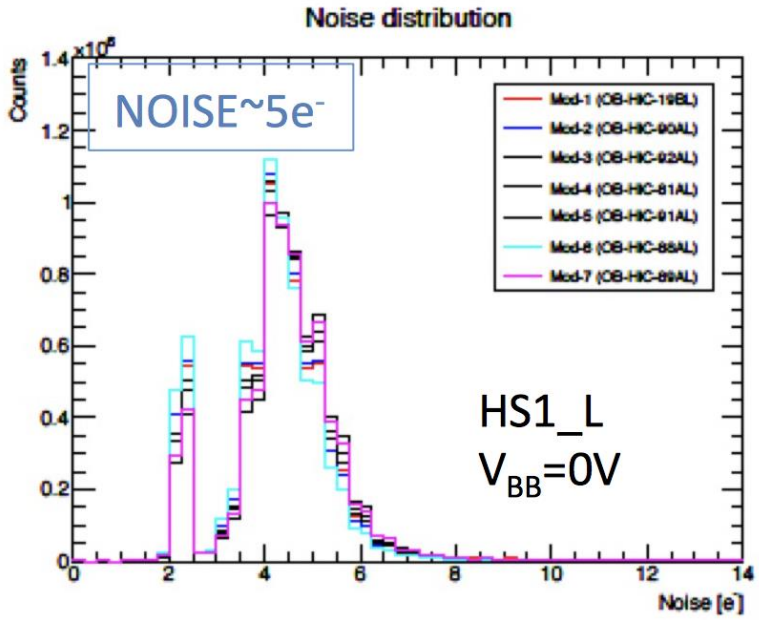
Stave Prototypes

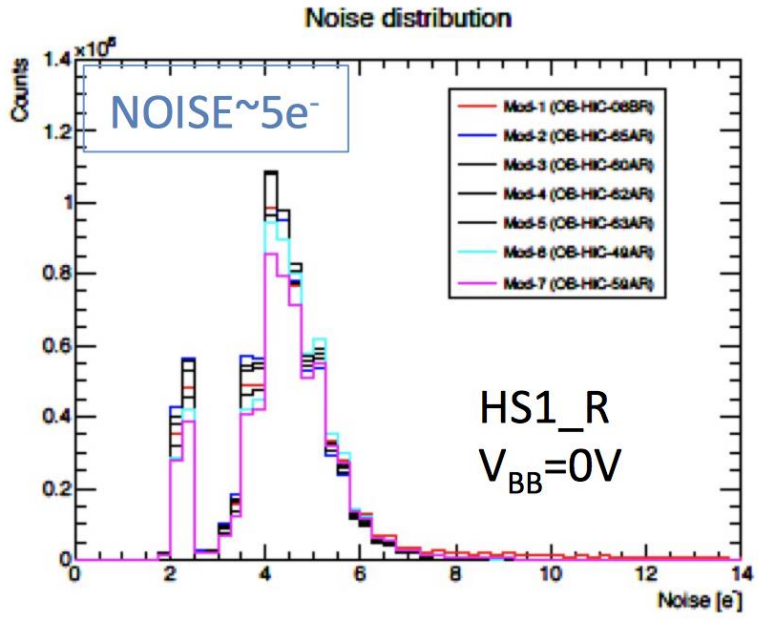
- Stave-0, Stave 1 and Stave 2 in Torino;
- ve-1:
  sured in threshold scan on all 98 chips operated
  e to single chips

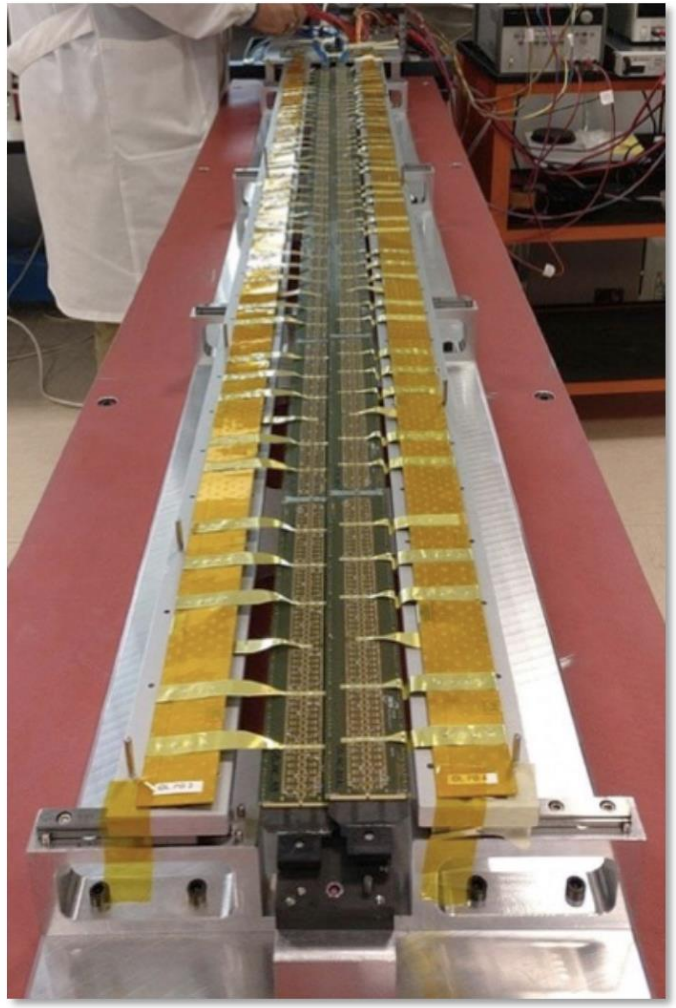
Biggest existing pixel detector scanned in ~ 1hour on laptop

102 Million pixel

Preliminary







Scans and Analyses

Scans

- All scans derived from one basic scan class
- Performs the actual measurement through identical interface for all scan types

Analyses:

- Scan specific data analysis (e.g. fitting of threshold curves)
- Writing of data files
- Reduction of data and writing of summary files
- Comparison of data with previous test stages (implementation ongoing)
- Generating of HIC classification based on configurable cuts
- Writing to DB

Output Data

Large data files

- Copied to eos (threshold fit results, digital scan hitmaps)

Result files

- Attached to database activity
- One file per scan and HIC
- Contains summary variables, usually per chip
- Contains scan conditions data:
  voltage and temperature measured on-chip, currents measured in power board, SW/FW version
- To be implemented: complete read-back of chip registers

Output variables

- Summary variables with lower granularity (usually per HIC) written as parameter to DB
- Allows direct reporting and easy monitoring of testing progress
- Would allow later revision of classification

Procedure

- User starts new test and selects test type
- The GUI prompts for location, user and HIC ID
- According to test type the software generates setup and test list
- The software tries to communicate with the chips and disables chips that do not answer

- The user enters some configuration options and starts the test
- The GUI runs the list of scans and analyses and prepare the results;
  this already creates the result objects and the local result files

- At the end of all scans the user can select to write to database
- In this case the software creates the database activity, attaches files and parameters and copies all local files to EOS

Software Status

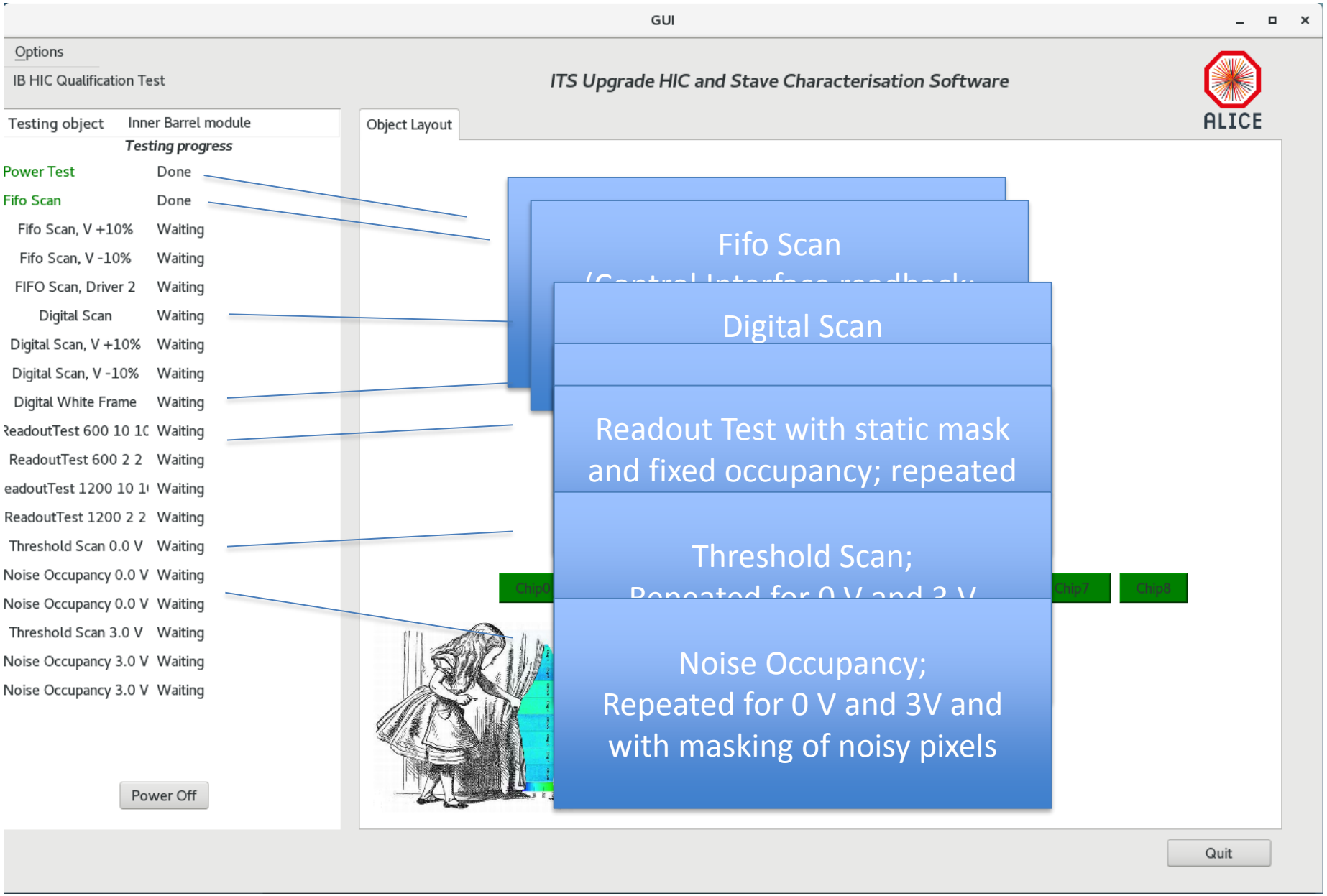
Software installed and running in all HIC sites
GUI routinely used for characterisation of newly assembled HICs

Main outstanding items:

- Definition of DB activities with parameters for remaining test stages (mainly endurance and half-stave test)
- Complete test of endurance and half-stave test
- Comparison of results with previous tests

- Several details on usability …

Software Status



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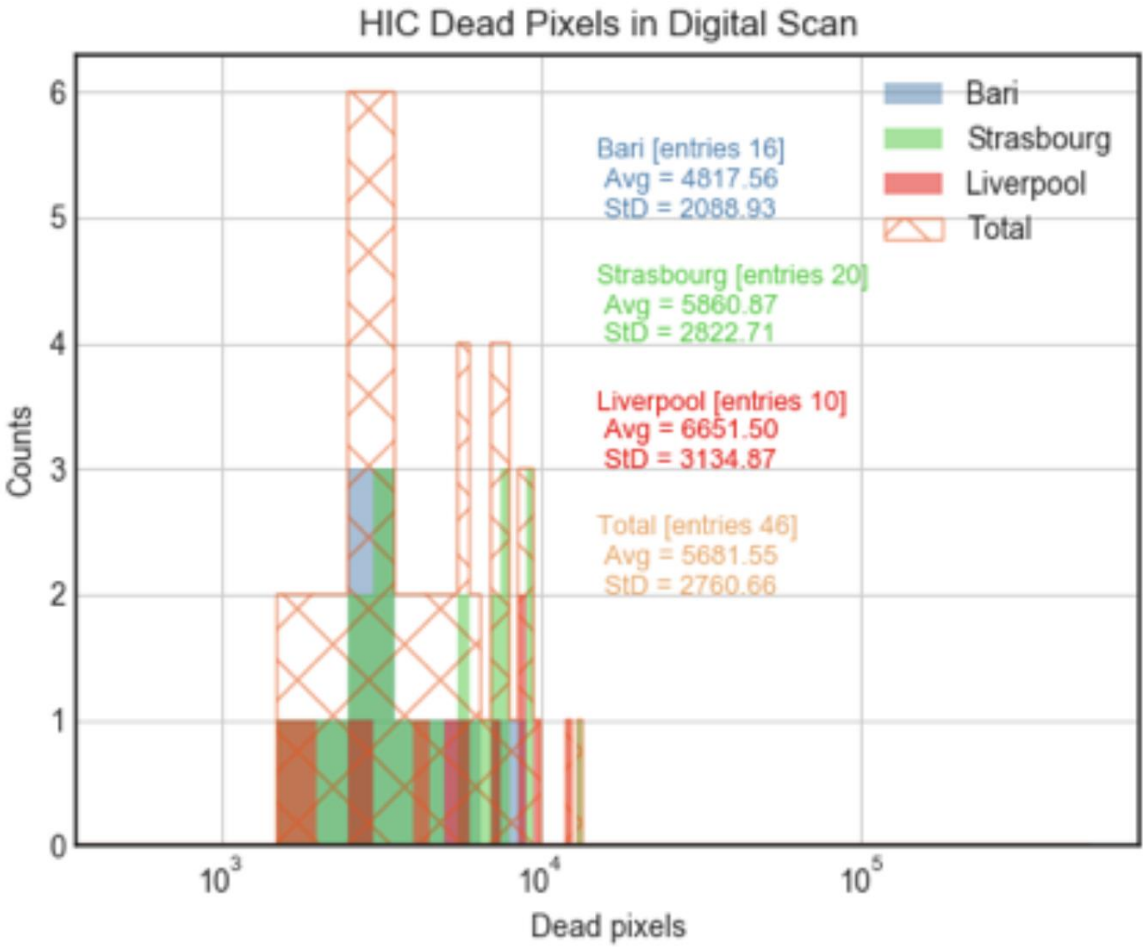
Progress and Quality Monitoring

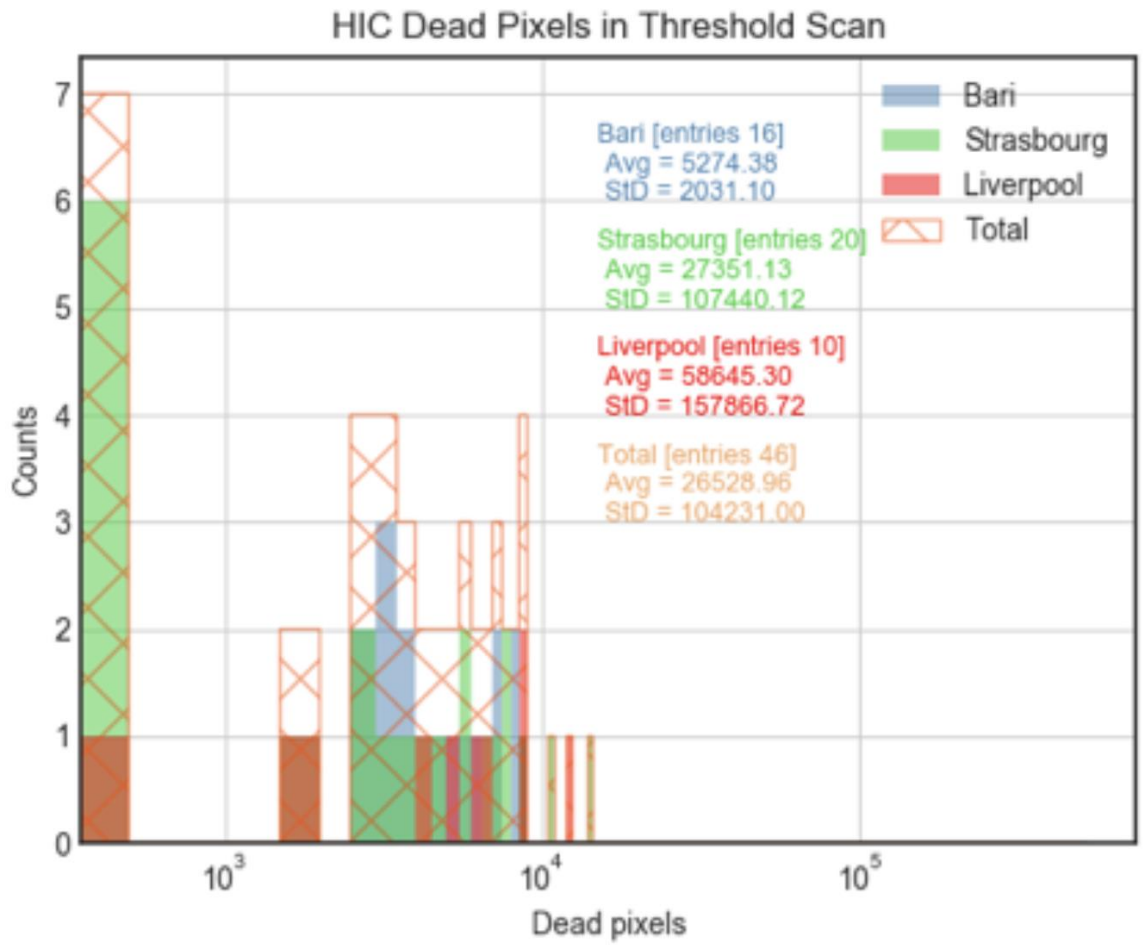
Several tools will be put in place to monitor the progress of the tests and help with possible problems (spotting and solving):

- Log files attached to database (ongoing)
- Config files attached to databases (done)
- Comparison with previous tests (ongoing)
- Reading back of chip config and writing into result files (ongoing)
- Main tool: preparation of reports from parameters in the database; will be prepared by Kybernetika.

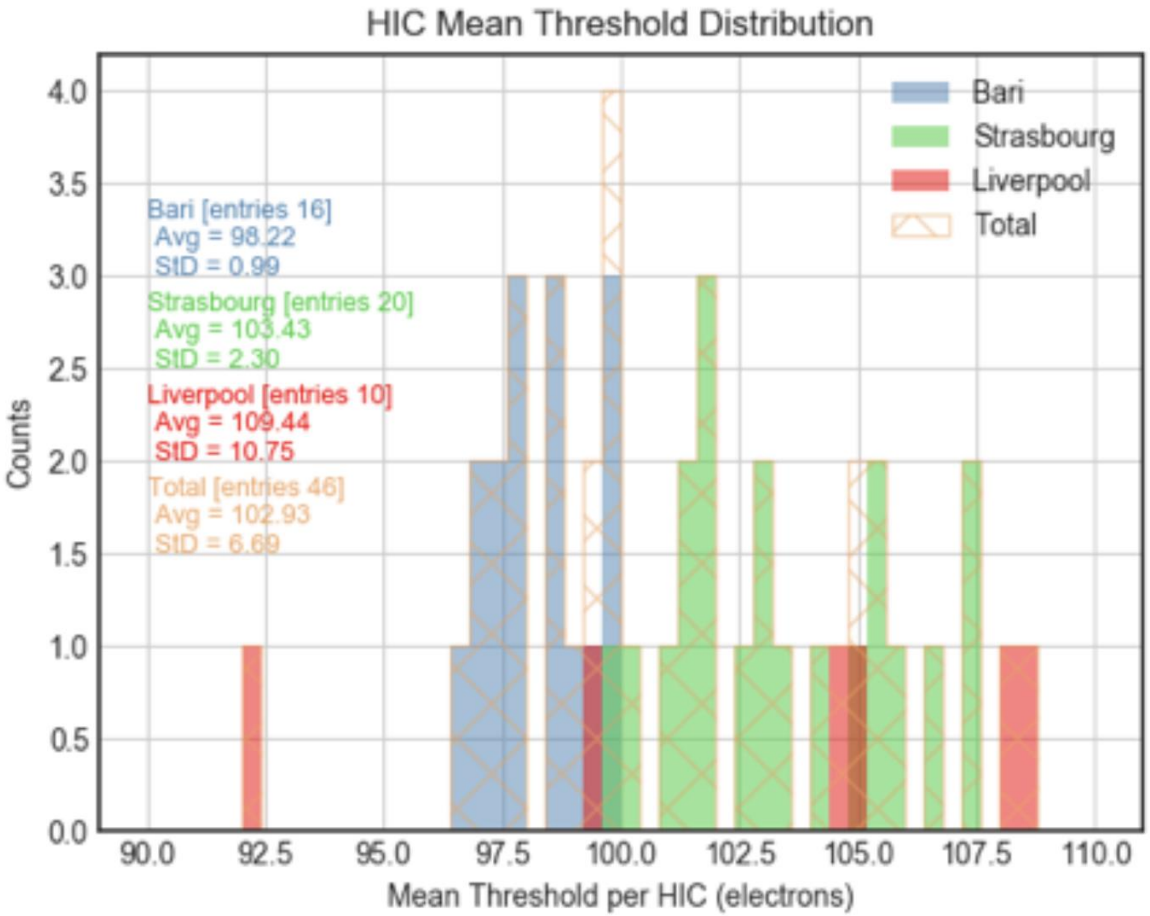
  Until this is in place prepare overview plots in manual way from database entries
  (next slides; thanks to Sergey and Domenico)
  These show nice consistent results, which are compatible with the experience from the chip tests

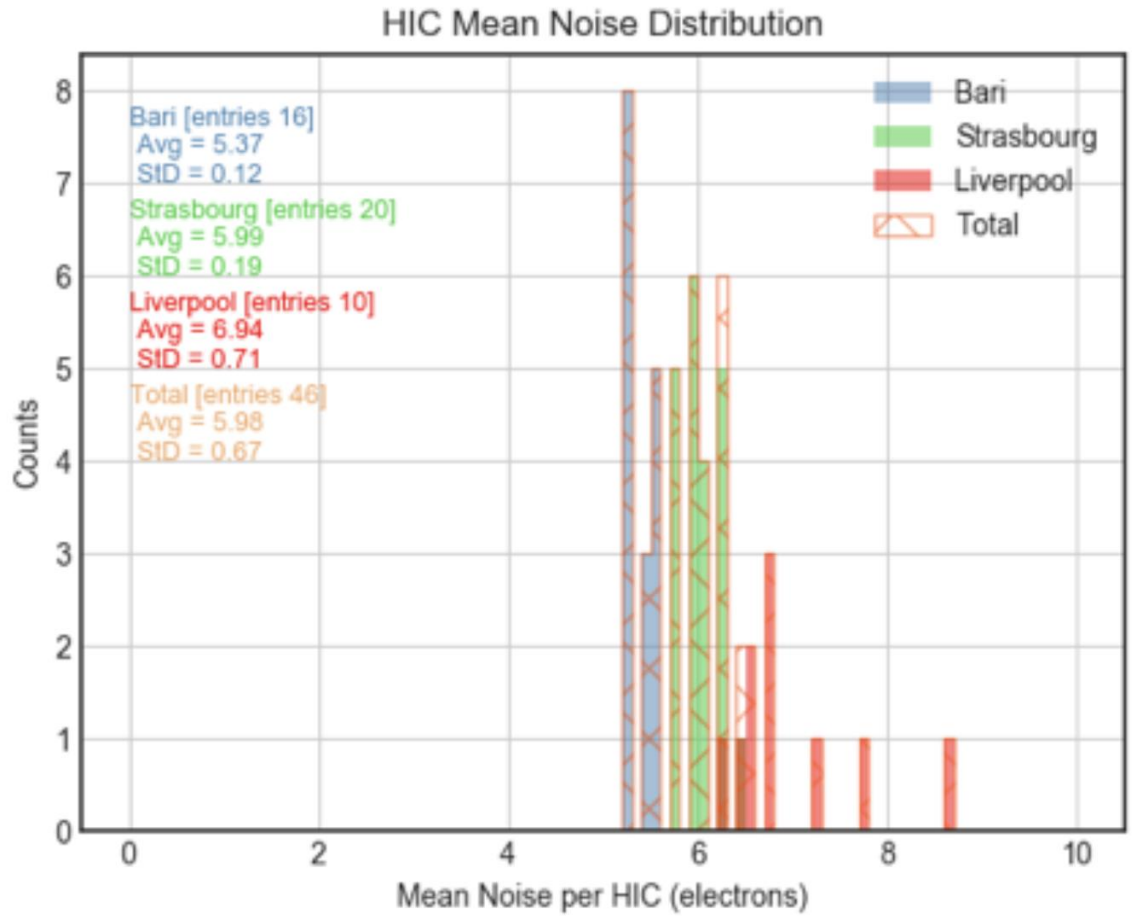
Progress and Quality Monitoring





Progress and Quality Monitoring





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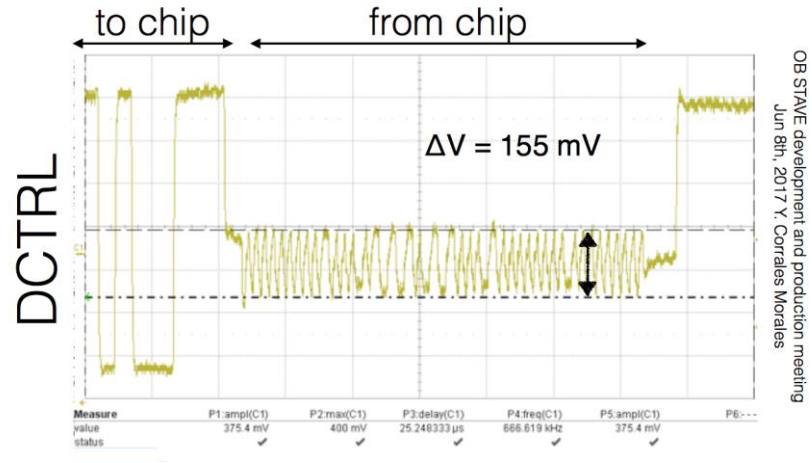
DCTRL Test

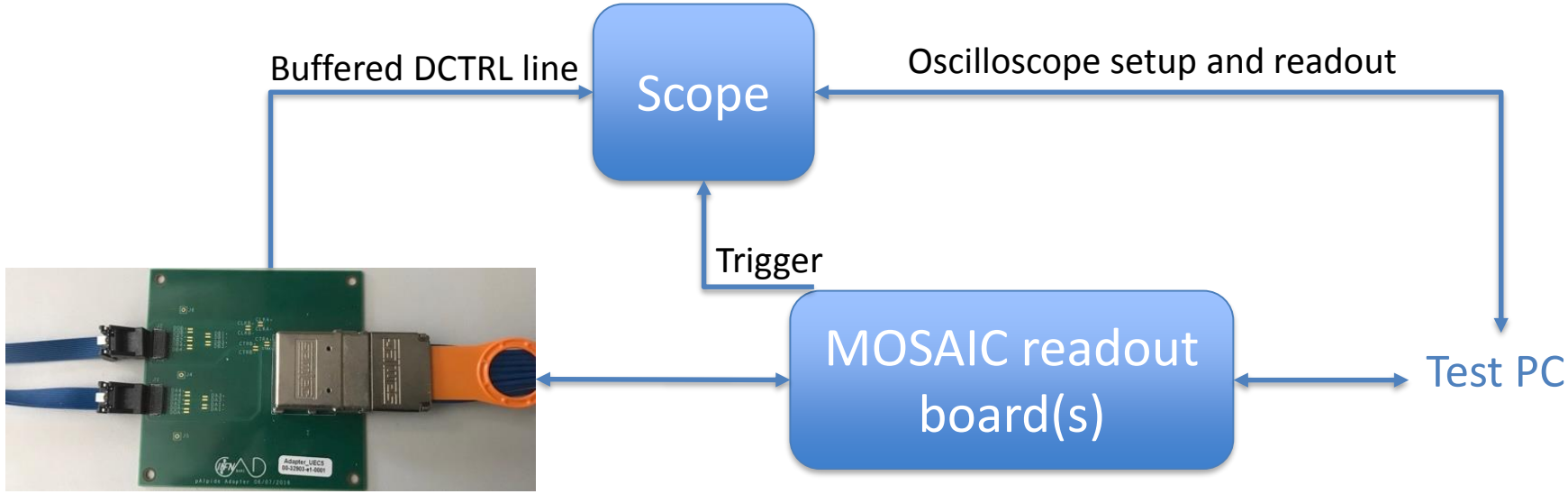
Goal: identify HICs with small margin in the DCTRL driver strength

- Already in place: CTRL readback at reduced driver strength
- Ongoing: implementation of direct measurement of signal amplitude



Setup:

- Modify adaptor board (adding of buffer and connector); design done
- Add oscilloscope to measure signal amplitude
- Modify MOSAIC firmware to trigger oscilloscope; done (timing on chip response)
- Test will be integrated into GUI (ongoing)

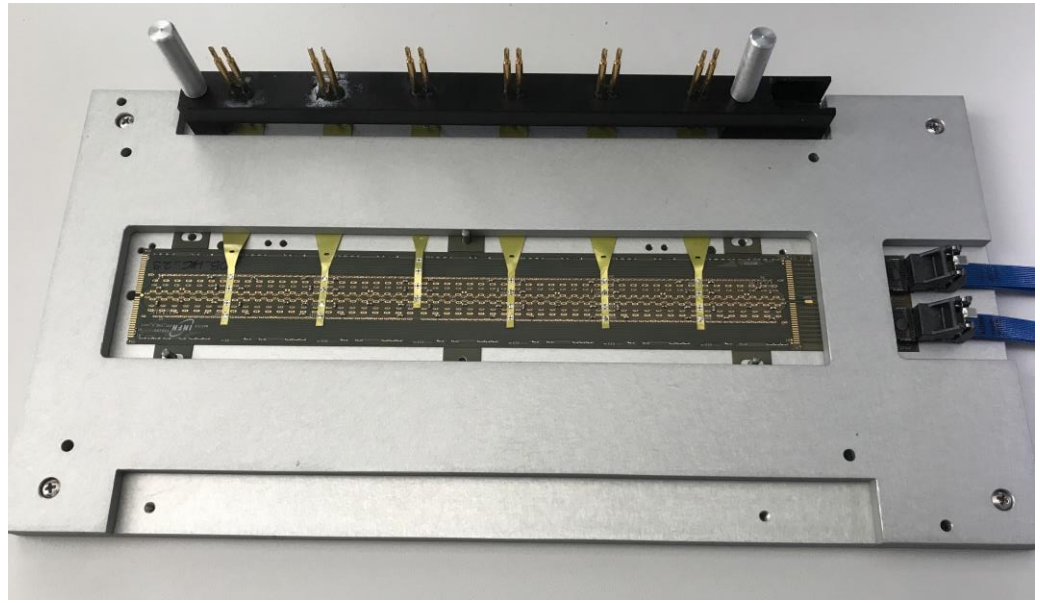


Powering Tests

Currently resistance routinely checked after assembly with Ohm-meter
Goal: implement a simpler and more consistent method

- Establish well-defined procedure with own activity in DB
  - Take I-V-curve over limited range
  - Save I-V-curve as attachment to activity
  - Save currents at e.g. 50 mV as parameter

- Setup: HIC with power adaptor on support plate. Connect with dedicated cable to programmable power supply



Summary

- A baseline test system – hardware and software – has been installed in the HIC sites
  Thank you all for your patience in installation and setting up!

- The software is fully functional and allows to perform lists of measurements in fully automated manner, analyse the data and write the results to the database

- First overview plots show nice consistent results, comparable to chip tests

- Next steps:
  - Complete database interaction, incl. reading of previous results
  - Finalise setups for endurance and half-stave tests
  - Add additional measurements
  - Iron out any problems and inconsistencies that might show up