HEAT TRANSFER USING ALUMINUM NITRIDE IN A SILICON MICROVERTEX DETECTOR

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Abstract

The Silicon Microvertex Detector (SMD) is a custom-designed instrument for physics research. More than 70,000 channels of electronics are densely packed on the SMD in an extremely confined volume. The SMD is subject to strict regulations regarding thermal management. To efficiently remove the heat generated by the electronics, both the ladder mounting hardware, and the electronics hybrid substrates were made from Aluminum Nitride.

THE SILICON MICROVERTEX DETECTOR

The Silicon Microvertex Detector (SMD) is a custom designed instrument used in a physics research experiment, L3, at the European Center for Particle Physics (CERN). The active sensing elements of the SMD are silicon microstrip sensors. Each sensor is comprised of hundreds of individual channels, called strips. The strip signals provide precise spatial coordinates of the track of an ionizing particle that has passed through the sensor volume . The position resolution of the strips is better than 10µm. The SMD is constructed from several different materials including silicon, quartz, carbon-fiber composite, and aluminum. In order to preserve the position resolution of the system, the temperature across the detector must be regulated and maintained.

The SMD is a two-layer, barrel type tracker (Figure 1.). The inner layer is at the approximate radius of 6cm from the beam, and the outer layer is at roughly 8cm. The SMD is comprised of 96 double-sided silicon sensors. A pair of sensors are daisy-chained into a structure called a half-ladder. Each half-ladder is an independent detection unit. There are 48 half-ladders in the SMD. The half-ladders are assembled by pairs into full ladders. The two halves of the full ladder are connected mechanically, but not electrically. The full ladder is the unit mechanical building block of the SMD. There are 24 full-ladders in the SMD.

The twelve ladders of the inner layer of the tracker are oriented parallel to the central axis of the SMD. These ladders overlap slightly at the edges in a shingled fashion. This helps to align the detector with particle tracks that pass through the overlapped region. The twelve outer ladders are oriented with a 2° tilt relative to the inner layer to help resolve tracking ambiguities. Both sides of the silicon sensors are readout to give a three-dimensional measurement of the charged particle tracks; R, Phi and Z.

The SMD covers the polar angle from 22° to 158°, and covers the full azimuth. The total number of individual channels, or strips that are readout on the SMD is 72,672.

THE SILICON SENSORS

The SMD silicon sensors are based on an INFN-Pisa design [1], and were fabricated at the Swiss Center for Electronics and Microtechnology (CSEM)[2]. Each of the sensors is approximately 4 x 7cm^2 and 300µm thick. Each strip on a side of the sensor functions as a diode, which, when operated under reverse bias collects the holes or electrons created along the track of an ionizing particle that has passed through the sensor volume. On one side, the strips are P-type and on the other they are N-type. The P-implantation strips run the length of the sensor, and are oriented parallel to the beam direction. These strips measure the Phi coordinate. The N-type strips are implanted on the opposite side of the sensor and are oriented orthogonal to the P-strips. These measure the Z coordinate; parallel to the beam direction. The readout pitch on the P-side is 50µm. The readout pitch on the N-side is 150 or 200µm, dependent on the polar angle location of the strip.

The strips are ac-coupled to the front-end electronics through 128 channel capacitor chips. The capacitors are polysilicon-polysilicon structures separated by a silicon dioxide layer, and fabricated on quartz substrates. The capacitor chips also have circuitry to protect each strip against transient high-current excursions.

FRONT-END ELECTRONICS AND HYBRID PROCESSING

The SMD front-end electronics readout chip is called the SVX-H. The SVX was designed by S. Kleinfelder et al. [3] at Lawrence Berkeley Laboratory (LBL) for the Collider Detector at Fermilab (CDF). The SVX-H is the radiation hardened version. An SVX is a 128 channel chip. A readout channel is comprised of a charge-sensitive amplifier, followed by a sample and hold stage, a comparator and latch, and digital logic to control the serial multiplexed output. The SVX can be operated in zero suppression mode, also referred to as sparse mode. This means that only the channels that were activated during a particular integration cycle will be output across the signal bus. The power dissipation of the SVX-H is about 175mW per chip. The SMD contains 576 SVX chips for a total estimated heat load in the front end of 100W.

There are several reasons why good thermal management is a central issue in the design and operation of the SMD. For one, the SMD is installed concentric into the inner-wall volume of another L3 detector, called the Time Expansion Chamber

(TEC). The calibration of the TEC is very sensitive to temperature changes in its operating gas volume. Before it was installed, it was agreed that the SMD could only be turned on and operated in the data-taking run if it did not affect the gas temperature of the TEC by more than 1° C. Clearly, in order to meet this requirement, the majority of the heat produced by the SVX's has to be removed.

Other cooling requirements are self-imposed by the SMD collaboration itself. The detection power of the SMD is the capability to give precise position-sensitive measurements. The gain in position resolution to the overall L3 experiment from SMD data is strongly dependent on the absolute and relative alignment of the detector, and on the long-term stability of that alignment. A great deal of design effort was spent to select and specify component materials that would be relatively stable with time and temperature. Amongst these material selections are the carbon-fiber cylindrical support structure, the carbon fiber/silicon-laminate stiffener rib on the ladder, and, of course, the AlN. But there is also material such as the aluminum in the support rings, where the CTE match to silicon or carbon fiber is less than ideal. Therefore, the most desirable situation is that the ambient temperature that the detector runs in, is not very different from the temperature at which it was assembled and surveyed. Also, temperature differences across the SMD should be as small as possible to avoid unwanted distortion or twists in the support structure or the ladder assembly. Lastly, for safe long-term operation of the SVX-H chip, we require that the operating temperature of the chip should not exceed 40°C.

The SVX die are mounted on multilayer hybrid circuit boards (see Figure 2.). Our circuit board design derives from work done by C. Haber et al. [4] for the CDF Experiment. The circuits are printed in a standard thick film process on Aluminum Nitride (AlN) substrates. AlN was chosen because of its excellent thermal conductivity; 180W/m-K, and because its CTE is well matched with that of silicon (Figure 3). Several firms are involved in the circuit buildup from raw material to completed hybrid.

The AlN blanks for the SMD were manufactured a Tokoyuma Soda[5] in Japan. They were shipped to Stellar Industries[6] in the US and lapped to our required thickness of 500µm and polished to a nominal surface finish of 0.5µm. The AlN plates were then sent to Questech[7], where they were laser scribed to our substrate dimensions. In order to facilitate the laser machining, Questech brings the substrate to an elevated temperature and places it on a heat stage. Coaxially-blown assist gases, consisting mostly of oxygen, are flowed over the substrate during the machining. The substrate is then cleaned and fired at a peak temperature of 950°C over an eight hour cycle to rid the surface of any residual organic compounds.

The scribed substrate plates were then sent to Promex[8] for thick-film printing. The complexity of our circuit design is such that our multilayer buildup requires 34 individual prints and 23 firings. The screening of the hybrids is done with metal and dielectric pastes that are specially formulated for compatibility with AlN. The pastes were developed by Ferro Corporation[9]. The metal or dielectric pastes are screened onto the substrate and allowed to air-dry for 10 to 20 minutes before they are passed through a 3-phase firing. The preheat is 50 to 60° C per minute ramp-up, followed by a 10 minute peak fire at 850° C, and a 40 to 50° C per minute cool down. There are more than 130 individual process steps associated with the circuit buildup. The biggest problem we encountered during the hybrid processing was associated with the pastes. The LBL team had found that the dielectric pastes they were using would begin to craze after multiple firings. Some of our prototype parts were also showing crazing in the dielectric and cracking and peeling around the vias, and blisters in the bond and solder pads. Ferro, aware of these problems, developed a new paste, part 2051, that had a better CTE match to the AlN. We printed some parts with the new dielectric, only to find that the adherence of the gold print to the dielectric was very poor. When we attempted to wire-bond to the pads, they were either completely obliterated or the pull strength was unacceptably low. Solder pads also did not adhere, and could be pulled up with a piece of adhesive tape. We decided to layer two of the older dielectrics that Ferro had produced, part numbers 10-050 and 10-154. We asked Promex to print the dielectric layer directly beneath all the bond and solder pads with the paste, 10-050, which exhibited known good adhesion characteristics, and to print all the other dielectric layers with the product, 10-054, which exhibited better behavior after multiple firings. The result was completely acceptable. Wire-bond pull strengths were greater than 8 grams on the bond pads, and the solder pad adhesion was solid. The final hybrid yield was better than 90% for a production run of 300 parts.

LADDER DESIGN

The basic mechanical building block of the SMD is called a ladder. A ladder is a complex assembly of electronic elements; silicon strips, coupling capacitors, and hybrid circuits, and mechanical elements; carbon-fiber composite stiffener and mounting hardware. Each ladder is built from two independent detector assemblies called half-ladders. The assembly sequence of the half-ladder is shown in Figure 4. Each of the approximately 20cm long half-ladders comprises two 7cm silicon sensors that are edge-glued with epoxy. The R-Phi strips on the P-side of a pair of sensors are connected by wire-bonding the corresponding strips across the glue joint, making 14cm long strips. The Z strips, on the opposite side of the sensors are oriented orthogonal to the R-Phi strips, and are wire-bonded to a thin kapton foil that is glued to the N-side of the sensor. The kapton foil is 50µm thick with 2.5µm of electroplated copper. The foil is etched to form a circuit that extends the Z strips to the end of the half-ladder via L-shaped traces. The circuit places the hybrids, which read out both sides of the sensor, at the end of the half-ladder. This is beneficial in several respects. The hybrid does not overlap the sensor and therefore does not degrade the detector resolution by scattering the incident particles. In addition, located at the ends, the heat generated on the hybrids is physically farther from the

silicon sensors. And lastly, the mechanics to remove the heat is simplified, making it possible to contact the hybrids of both sides of the sensor with one cooling ring.

The hybrids are made into assemblies called electronics units. An electronics unit is comprised of a P-side hybrid, an N-side hybrid, and their associated coupling capacitor assemblies. The capacitor assemblies are glued to, and separated by a thin quartz plate, called the thermal break. The quartz thermal break puts a high impedance path between the hybrid electronics and the silicon sensors. The results of finite element simulations indicated to us that this thermal isolation helps to keep the silicon sensors close to room temperature, under nominal operating conditions.

The pair of hybrids are glued to, and separated by a thin AlN plate, called the thermal tongue. The thermal tongue extends 10mm aft of the hybrids. It serves two important functions. It is the mounting ear for the ladder, defining the precise location of the ladder to the support rings (which are also the cooling rings). It is also a low impedance thermal path for the heat to flow to the cooling rings. The thermal tongue is built up from three pieces of AlN which are glued with conductive epoxy to preserve good thermal conduction. There are four types of tongue in the SMD. Two are specifically designed for the outer layer ladders and two for the inner layer. Two half-ladders become a full ladder when they are joined silicon to silicon, with the half-ladder electronics units located at opposite extremities. On one end of the ladder, the locators are precision machined holes. These are diamond-bit-milled to +9μm/-0 tolerance[11]. On the opposite end, the locators are slotted to allow for thermal expansion of the ladder. On each end, only one of the slots or holes is a precise locator (Figure 5.).

THE COOLING SYSTEM

The total heat generated by 96 hybrids in the front-end electronics of the SMD is ~100w. We chose water cooling to remove this heat load from the detector volume. The support rings that the ladders are mounted to contain a water cooling channel, 1mm high by 10mm wide. The small aspect ratio of the width to the height maximizes the thermal contact area between the water and the aluminum wall. The cooling channels were machined into the aluminum support rings by an electro-erosion process, and then the channel walls were resealed by electron beam welding.

The AlN hybrids and the AlN thermal tongue provide a good thermal conduction path from the heat source to the cooling rings. And yet, finite element simulations indicated that the temperatures at the chip level, and at the silicon would exceed our proposed limits, that is, 40° maximum for the chip, and near room temperature at the silicon. The solutions suggested that an additional thermal path was necessary, and that it must be located as close as possible to the heat source. Fortunately, during the design phase of the hybrids, we anticipated in spirit, if not in detail, the potential need for such a contact. We bunched the passive surface mount components on the hybrid as close as possible, leaving a 5mm rectangular strip across the entire width of the hybrid free of components. A solid mechanical connection to this area was out of the question, as this would compromise the kinematical support of the ladders. The cooling ring was subsequently designed, so that upon assembly to the support structure, this rectangular area was positioned directly above a machined flat on the ring. The gap between the flat and the hybrid was made 500μm. Several "soft" thermally conductive materials were evaluated to fill this gap. In the end, we chose to make the thermal path with conductive grease. Several products were tested. Dow Corning 340 silicone compound[10] was chosen on the basis of its thermal conductivity, which we measured to be 1.25W/m-K, and because of its long term high viscosity characteristics. The finite element model predicts that more than 50% of the heat generated on the hybrids is taken out through the thermal grease path. The remainder is channeled through the aft connection made by the AlN thermal tongue to the cooling ring.

The thermal model that we had run, assumed 18°C water in the cooling rings. Both a nominal and worst case solution were input. The worst case solution de-rated the grease thermal conductivity, and the integrity of the thermal tongue contact. The chip temperature was predicted to be 34.7°C in the worst case, and 28.4°C for the nominal solution (Figure 6). The temperature at the cooling ring was predicted to be 21°C. The actual mean temperature of the input water to the cooling rings in 1994 is 13°C. The results of the data collected from temperature sensors that are mounted on the SMD, taken form a running period of 120 days in the 1994 data run, is plotted in Figure 7. The Mout temperature sensor is located in the middle of the support structure, on the outer layer, directly beneath a silicon sensor. The Min sensor is located in an analogous position on the inner layer. The lower sets of data points are the averages of 6 sensors that are located on the support structure, directly below the SVX, and adjacent to the cooling rings on the inner and outer layers. Accounting for the -3°C shift between the actual and assumed temperature of the input water to the cooling rings, the temperatures measured at mid-support, ~19°C, and the temperatures measured near the cooling rings, ~16°C, are consistent with the predictions of the thermal model. The temperature at the silicon is acceptably close to the assembly temperature. And although we don't have a thermal sensor attached directly to the SVX chip, the 16°C reading that we record just below the chip is a strong indicator that the chip surface is running well below 40°C.

CONCLUSION

Because of its high thermal conductivity and good CTE match with silicon, AlN is an excellent substrate material for high density electronics. Complex multilayer circuitry can be printed on AlN, using a standard thick film process, however, further

research in the development of AlN compatible pastes is warranted. Finite element modeling provides valuable information tc guide the development of a reliable cooling system.

References

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[10] Dow Corning Corp., Midland, Mi., USA
[11] Piguet Freres, Le Brassus, Switzerland

Fig. 1. - The SMD on a metrology stage.

Fig. 2. - A close-up of the Z-side of a ladder.

Fig. 3. - Table of material properties.

Fig. 4. - Assembly sequence of a half-ladder.

Fig. 5. - The mounting hardware.

Fig. 6. - Thermal model results.

Fig. 7. - 1994 temperature data.

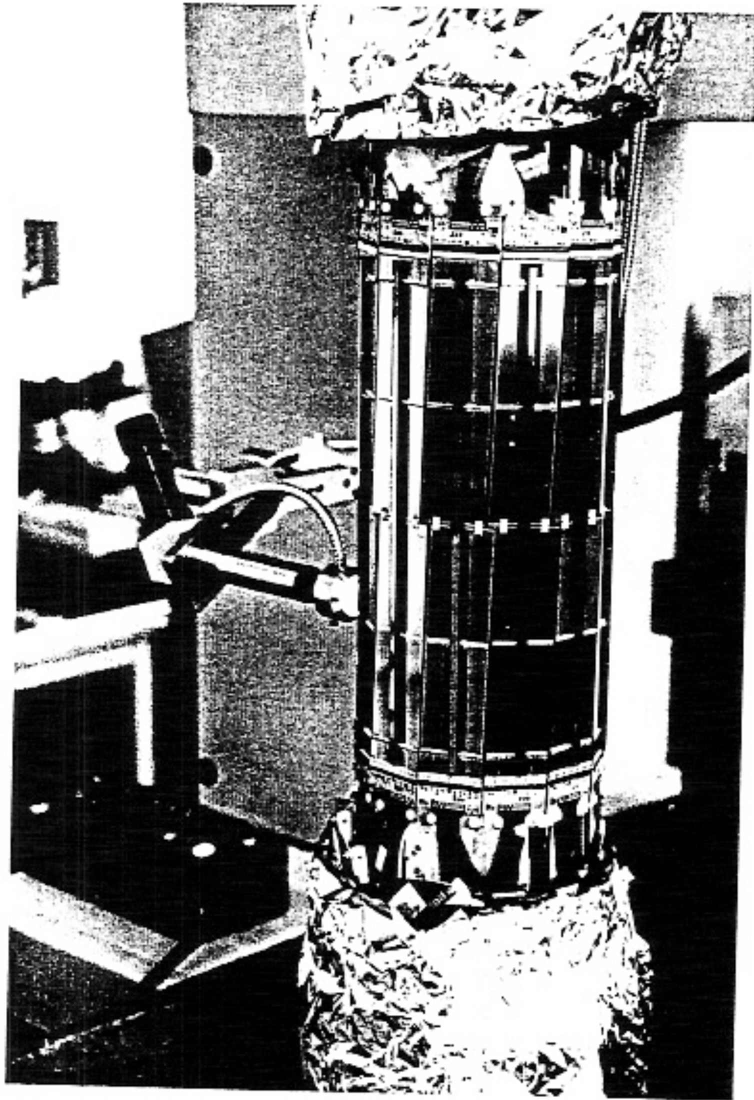


Figure 1.

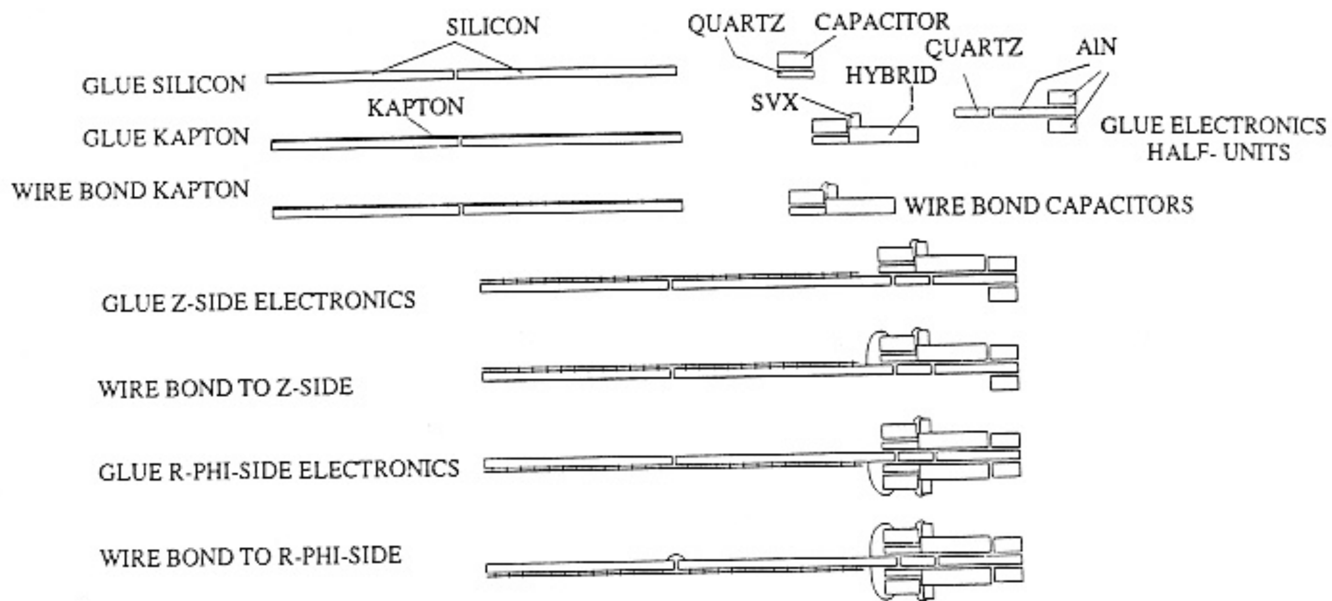


Figure 4.

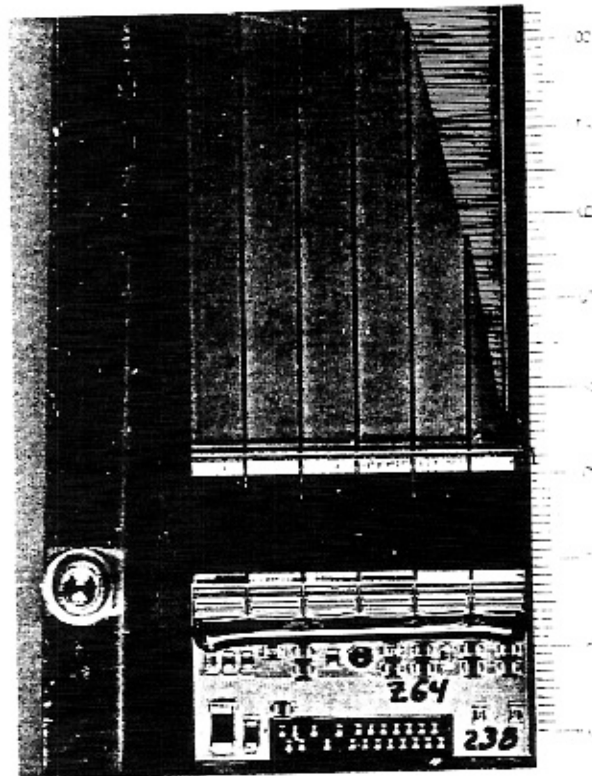


Figure 2.

ELECTRONIC SUBSTRATE MATERIALS PROPERTIES

Properties	UNITS	Al_2O_3	BeO	AlN
Thermal Conductivity	(W/m-K)	15-20	270-300	100-220
Thermal coefficient of expansion	$(10^{-6}/C)$	7.2	8.3	4.3
Dielectric Constant	NA	9.4	6.5	8.6
Volume Resistivity	Ω-cm	$>10^{14}$	$>10^{15}$	$>10^{13}$

* CTE OF SILICON = 2.6 10^{-6}/C

THERMAL CONDUCTIVITY OF SILICON = 129 (W/cm-K)

Figure 3.

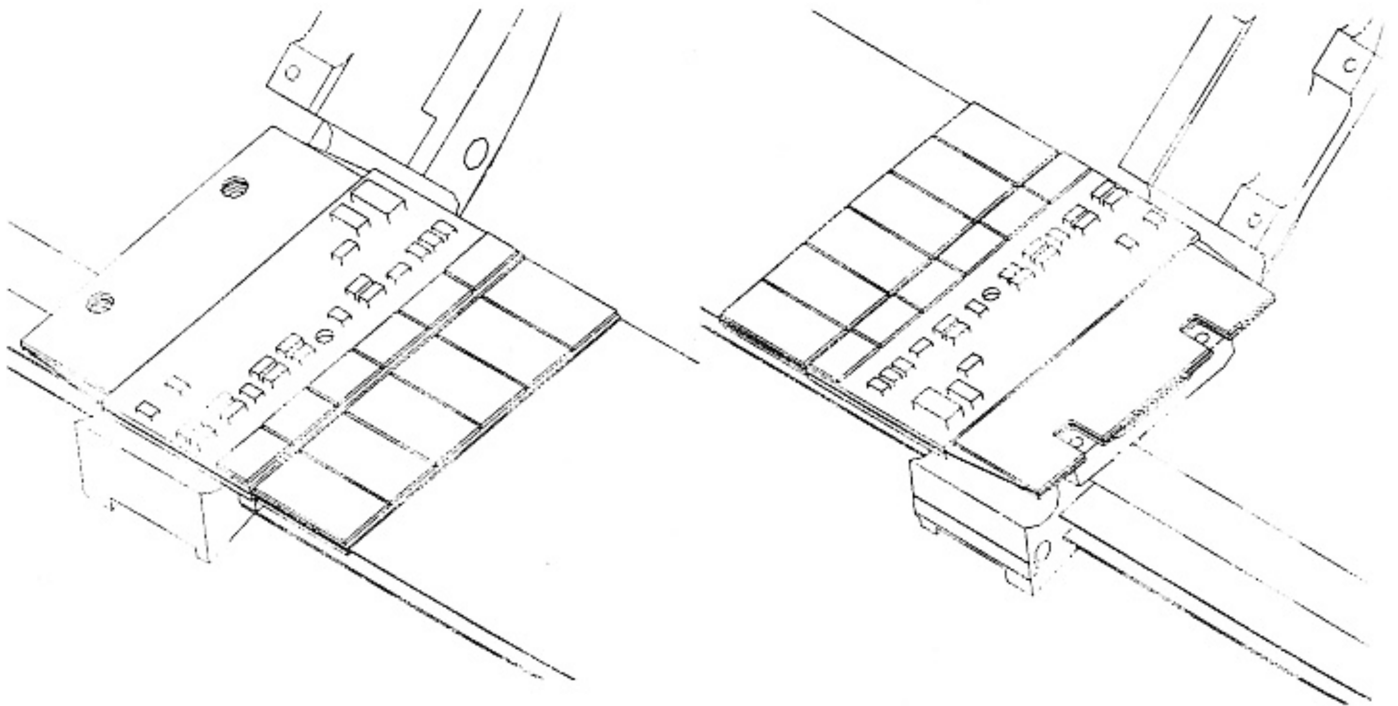
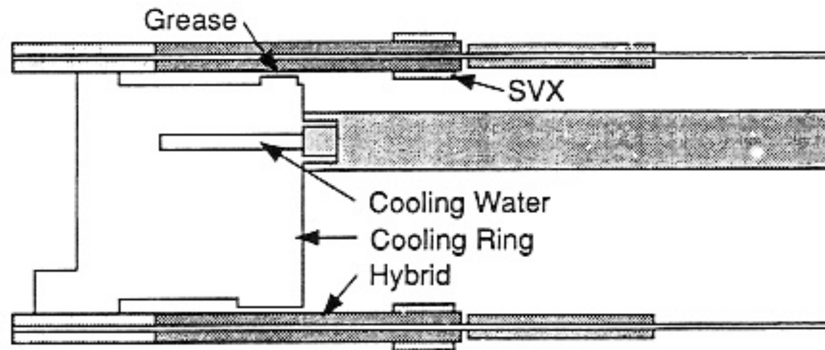


Figure 5.

Electronic Cooling ΔT's



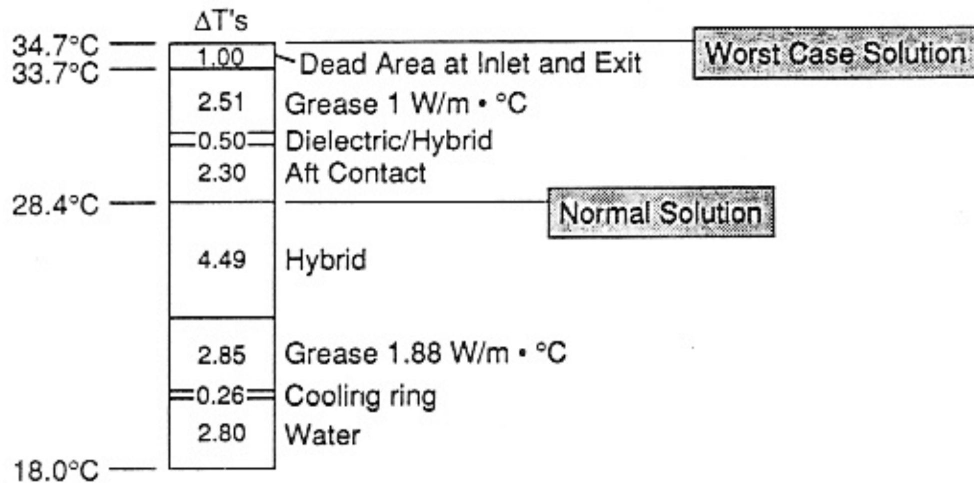
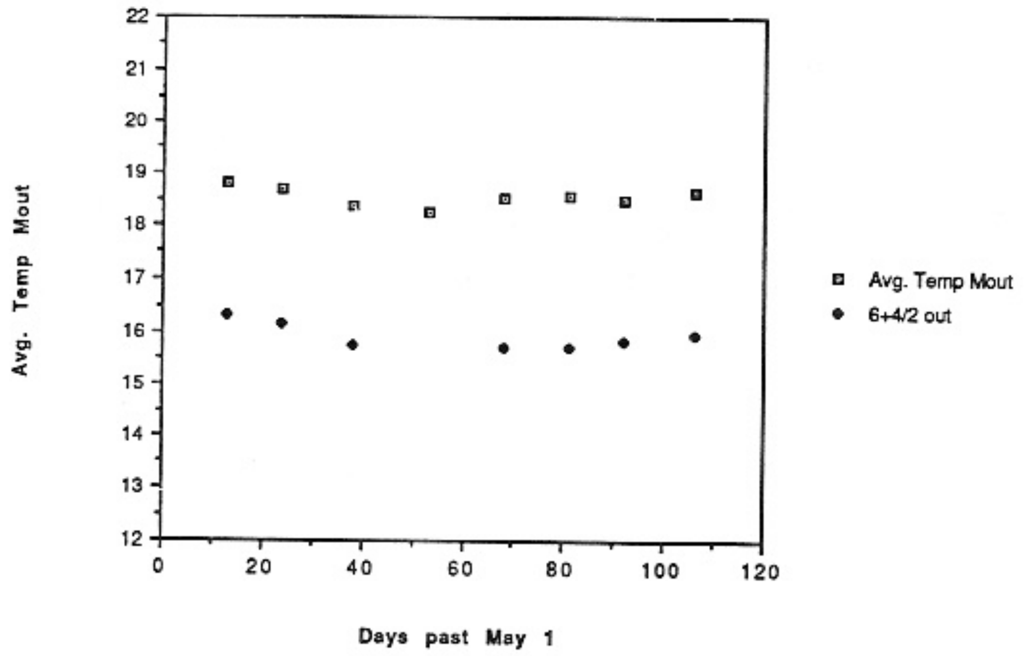


Figure 6



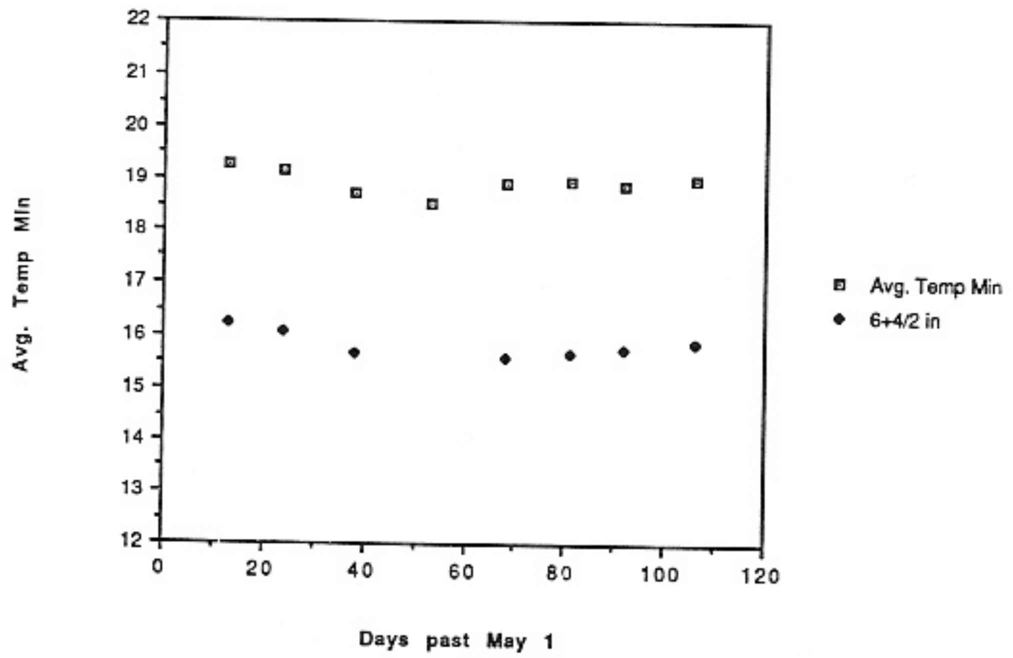


Figure 7