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Muon Tracker Preamp User's Data Sheet

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This document describes the Muon Tracker Charge Pre-amp (CPA) Application Specific Integrated Circuit (ASIC). Pin definitions are listed along with function and typical voltages. Mechanical information of the package is included to allow for accurate circuit board layout.

This document is based entirely on the earlier work of Mark Musrock and John Halliwell, formerly of Oak Ridge National Laboratory.

1 Introduction

The CPA chip is 8 channels of charge sensitive amplifiers followed by shaping amplifiers. The design allows for test input pulse signals to be generated on chip by an on-chip DAC which sets the level for the test pulses. Individual channels can be disabled via the serial data string.

2 Pin Definitions.

Table 1 below describes the pin out of the CPA chip. The first column identifies the pin number of the QFP package. The second column contains the wire bond pad number of the die for reference purposes. The pin name and description then complete the table.

Table 1. Pin Definitions

Package Pin No.	IC Pad No.	Pin Name	Description
1		GND	Ground for Package Floor. Pre-GND
2		NC	NC
3		NC	NC
4		NC	NC
5	18	Vss-pre	Vss for Preamp. Pre-GND
6	19	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
7	20	Qin-1	Channel 1 input.
8	21	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
9	22	Qin-2	Channel 2 input.
10	23	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
11	24	Qin-3	Channel 3 input.
12	25	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
13	26	Qin-4	Channel 4 input.
14	27	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
15	28	Qin-5	Channel 5 input.
16	29	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
17	30	Qin-6	Channel 6 input.
18	31	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
19	32	Qin-7	Channel 7 input.
20	33	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
21	34	Qin-8	Channel 8 input.
22	35	Vdd-pre	Vdd for Preamp. Pre-Vdd +5V
23	36	Vss-pre	Vss for Preamp. Pre-GND
24	37	Vdd-dig	Vdd for Digital. Digital-Vdd +5V
25	38	Vss-dig	Vss for Digital. Digital-GND
26	39	SD-IN	Serial Data input. TTL
27		NC	NC
28		NC	NC

29		NC	NC
30		GND	Ground for Package Floor. Pre-GND
31		GND	Ground for Package Floor. Pre-GND
32		NC	NC
33	40	Vss-Shaper	Vss for Shaper. Shaper-GND
34	41	Vdd-Shaper	Vdd for Shaper. Shaper-Vdd +5V
35	42	Reset-Out	Output monitor. TTL. (NOT used to daisy chain to next channel.)
36	43	DCLK-Out	Data clock output monitor. (NOT used to daisy chain to next channel.) TTL
37	44	Readback-Out	Output monitor of Readback signal. TTL. (NOT used to daisy chain to next channel.)
38	45	SCLK-Out	Serial Data Clock buffered output. (NOT used to daisy chain to next channel.) TTL
39	46	Vss-dig	Vss for Digital. Digital-GND
40	47	Inj-Bar	Control line for charge injector capacitor. TTL. Low = INJ-BAR, High = Vdd.
41	48	Vss-dig	Vss for Digital. Digital-GND
42	49	Vdd-dig	Vdd for Digital. Digital-Vdd +5V
43	50	Vmid	Mid-rail bias input. Typical +2.5V
44	51	Reset-In	Serial Register Reset. Active high. TTL
45	52	DCLK-In	Data clock input. TTL
46	53	Read back-In	Readback control input. TTL
47	54	SCLK-In	Serial shift clock input. TTL
48	55	SD-OUT	Serial Data output. (NOT used to daisy chain to next channel.) TTL
49		NC	NC
50		GND	Ground for Package Floor. Pre-GND
51		GND	Ground for Package Floor. Pre-GND
52		NC	NC
53		NC	NC
54		NC	NC
55	56	Vdd-Shaper	Vdd for Shaper. Shaper-Vdd +5V
56	57	Vss-Shaper	Vss for Shaper. Shaper-GND
57	58	DAC-rfb-bias	Bias point for op-amp amp-dac-p2x & amp-dac-p10x. Nominally 3.867 V.
58	59	DAC-inj-bias	Bias point for op-amp amp-dac-p2x & dac-pre-fb-cal. Nominally 3.867 V.
59		NC	NC
60	60	Output-8	Channel 8 output
61		NC	NC
62	61	Output-7	Channel 7 output
63		NC	NC
64	62	Output-6	Channel 6 output
65		NC	NC
66	1	Output-5	Channel 5 output
67		NC	NC
68	2	Output-4	Channel 4 output
69		NC	NC
70	3	Output-3	Channel 3 output
71		NC	NC
72	4	Output-2	Channel 2 output
73		NC	NC

DRAFT

74	5	Output-1	Channel 1 output
75	6	Vdd-Shaper	Vdd for Shaper. Shaper-Vdd +5V
76	7	Vss-Shaper	Ground for Package Floor. Pre-GND
77		NC	NC
78		NC	NC
79		NC	NC
80		GND	Ground for Package Floor. Pre-GND
81		GND	Ground for Package Floor. Pre-GND
82		NC	NC
83	8	Vss-dig	Vss for Digital. Digital-GND
84	9	Vdd-dig	Vdd for Digital. Digital-Vdd +5V
85		NC	NC
86	10	Off-DAC	Offset DAC monitor/external override. 0.1uF Bypass capacitor.
87	11	Vmid	Mid-rail bias input. Typical +2.5V
88		NC	NC
89	12	R4BS-bias	Bias monitor/external input for R4BS op-amps in shaper circuit. Referenced to Vdd-shaper.
90		NC	NC
91	13	Bias-rfb	Bias monitor for integrator resistive reset MOSFET gate
92		NC	NC
93	14	Char-bias	Monitor pin for Charge amp. Also used to externally control charge pre-amp bias. Reference to Vdd-pre.
94		NC	NC
95	15	INJ-LEV	Monitor for injection level control. Allows external monitor or external injection. Use with bypass capacitor.
96		NC	NC
97	16	Vdd-Shaper	Vdd for Shaper. Shaper-Vdd +5V
98	17	Vss-Shaper	Vss for Shaper. Shaper-GND
99		NC	NC
100		GND	Ground for Package Floor. Pre-GND

3 Package Information

The production CPA chip is packaged in a plastic molded 100-pin quad flat pack (QFP) package. Lead pitch is 0.65 mm with a footprint size of 3.2 mm. The needed package body thickness is 2.7 mm in order to ensure compatibility with the prototype ceramic packages. Expected cost of this package will be significantly less than $2.00 each in quantity.

ASAT QFP Package

EXTERNAL LEAD PITCH	1.0 MM	0.8 MM	0.65 MM	0.5 MM	0.4 MM
BODY SIZE	**LEAD COUNT**				
14.0 MM X 20.0 MM Thickness: 2.0mm - Footprint: 3.2mm Thickness: 2.7mm - Footprint: 3.2mm, 3.9mm	64	80	100	120* 128*	-

* Available in 2.7mm Thickness at this time.

ASAT PACKAGES THERMAL RESISTANCE DATA

PACKAGE	BODY SIZE (mm)	Mold Comp.	Die Paddle Size (mils)	Die Size (mils)	Theta J-A (C/W) Air Flow (ft/min)					Theta J-C (C/W)
					0	100	200	400	600	
MQFPs										
100L ED	14x20x2.7	6710SJ		250x250	27	23	20	17.6	15	1.31
100L STD	14x20x2.0	6710SJ	260x260	200x200	42	36.5	34	31.5	30	11.7

Package Dimensions will eventually be found at http://www.asat.com/html/drawing-files.html. Until this site is operational, the following URL has dimensions that accurately describe this package: http://www.nsc.com/packaging/mkt/vce100a.pdf.

4 Serial Data String Definition

Table 2 shows the serial data string consists of the following bits required for configuration of the CPA chip. There are a total of 34 bits. These are listed in the order of loading, Bit 0 loads first, bit 33 loads last.

Table 2. Serial Data Bits - Order and Function.

Bit No.	Name	Function	Bit No.	Name	Function
0	Off_dac_bit5	Output Offset Control Bit 5 (MSB) [default = 0]	17	Rfb_dac_bit0	Preamp baseline restore DAC bit 0 (LSB) [default = 1]
1	Off_dac_bit4	Output Offset Control Bit 4 [default = 1]	18	Pre_res_chan8	Channel 8 Preamp reset bit [default = 0]
2	Off_dac_bit3	Output Offset Control Bit 3 [default = 1]	19	Pre_res_chan7	Channel 7 Preamp reset bit [default = 0]
3	Off_dac_bit2	Output Offset Control Bit 2 [default = 1]	20	Pre_res_chan6	Channel 6 Preamp reset bit [default = 0]
4	Off_dac_bit1	Output Offset Control Bit 1 [default =1]	21	Pre_res_chan5	Channel 5 Preamp reset bit [default = 0]
5	Off_dac_bit0	Output Offset Control Bit 0 (LSB) [default = 0]	22	Pre_res_chan4	Channel 4 Preamp reset bit [default = 0]
6	Inj_dac_bit5	Injection level DAC bit 5 (MSB) [default = 0]	23	Pre_res_chan3	Channel 3 Preamp reset bit [default = 0]
7	Inj_dac_bit4	Injection level DAC bit 4 [default = 0]	24	Pre_res_chan2	Channel 2 Preamp reset bit [default = 0]
8	Inj_dac_bit3	Injection level DAC bit 3 [default = 0]	25	Pre_res_chan1	Channel 1 Preamp reset bit [default = 0]
9	Inj_dac_bit2	Injection level DAC bit 2 [default = 0]	26	Pre_inj_chan1	Preamp inject enable channel 1 [default = 0]
10	Inj_dac_bit1	Injection level DAC bit 1 [default = 0]	27	Pre_inj_chan2	Preamp inject enable channel 2 [default = 0]
11	Inj_dac_bit0	Injection level DAC bit 0 (LSB) [default = 0]	28	Pre_inj_chan3	Preamp inject enable channel 3 [default = 0]
12	Rfb_dac_bit5	Preamp baseline restore DAC bit 5 (MSB) [default = 1]	29	Pre_inj_chan4	Preamp inject enable channel 4 [default = 0]
13	Rfb_dac_bit4	Preamp baseline restore DAC bit 4 [default = 0]	30	Pre_inj_chan5	Preamp inject enable channel 5 [default = 0]
14	Rfb_dac_bit3	Preamp baseline restore DAC bit 3 [default = 0]	31	Pre_inj_chan6	Preamp inject enable channel 6 [default = 0]
15	Rfb_dac_bit2	Preamp baseline restore DAC bit 2 [default = 0]	32	Pre_inj_chan7	Preamp inject enable channel 7 [default = 0]
16	Rfb_dac_bit1	Preamp baseline restore DAC bit 1 [default = 0]	33	Pre_inj_chan8	Preamp inject enable channel 8 [default = 0]

5 Operation of Serial Data Registers

Figure 1 shows the serial register architecture for loading and readout of the serial data. This architecture is consistent with that used for several other custom integrated circuits being developed ORNL for PHENIX.

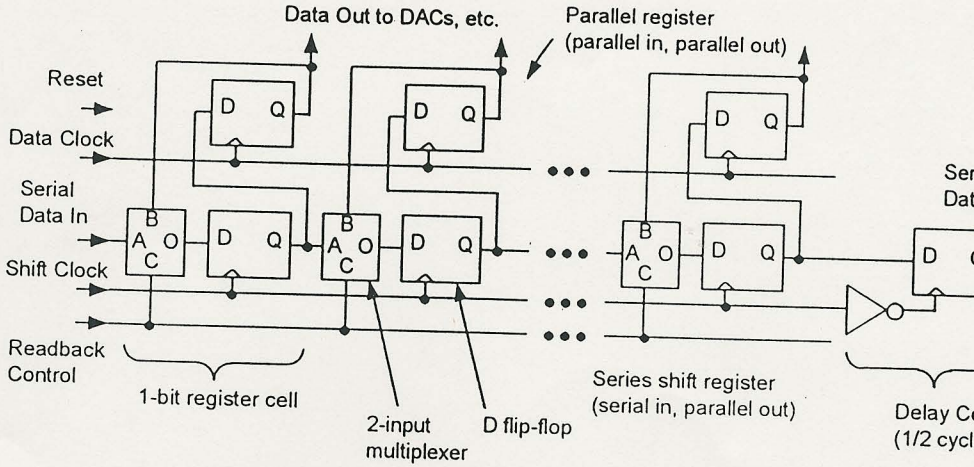

Figure 1. Serial data register architecture.

Serial data loads into the Serial Data In line with the positive edges of the Shift Clock signa data is loaded into the Parallel register with a single rising edge of Data Clock. Readback Control is low when loading data. Verification of the loaded data is done by setting Readback control high, tog Data Clock once to load a copy of the data register into the series shift register, and then clock out th with the serial Shift Clock.

6 Operating Conditions

Table 3 shows supply and external biasing voltages required for normal operation of the CPA chip.

Table 3. Required voltages.

Pin(s) Name	Function	Value
Vdd-pre	Voltage supply for pre-amps	+5V dc
Vss-pre	Ground for pre-amps	0V
Vdd-shaper	Voltage supply for shaper circuits	+5V dc
Vss-shaper	Ground for shaper circuits	0V
Vdd-dig	Voltage supply for digital circuits	+5V dc
Vss-dig	Ground for digital circuits	0V
Vmid	Bias voltage	2.5V dc

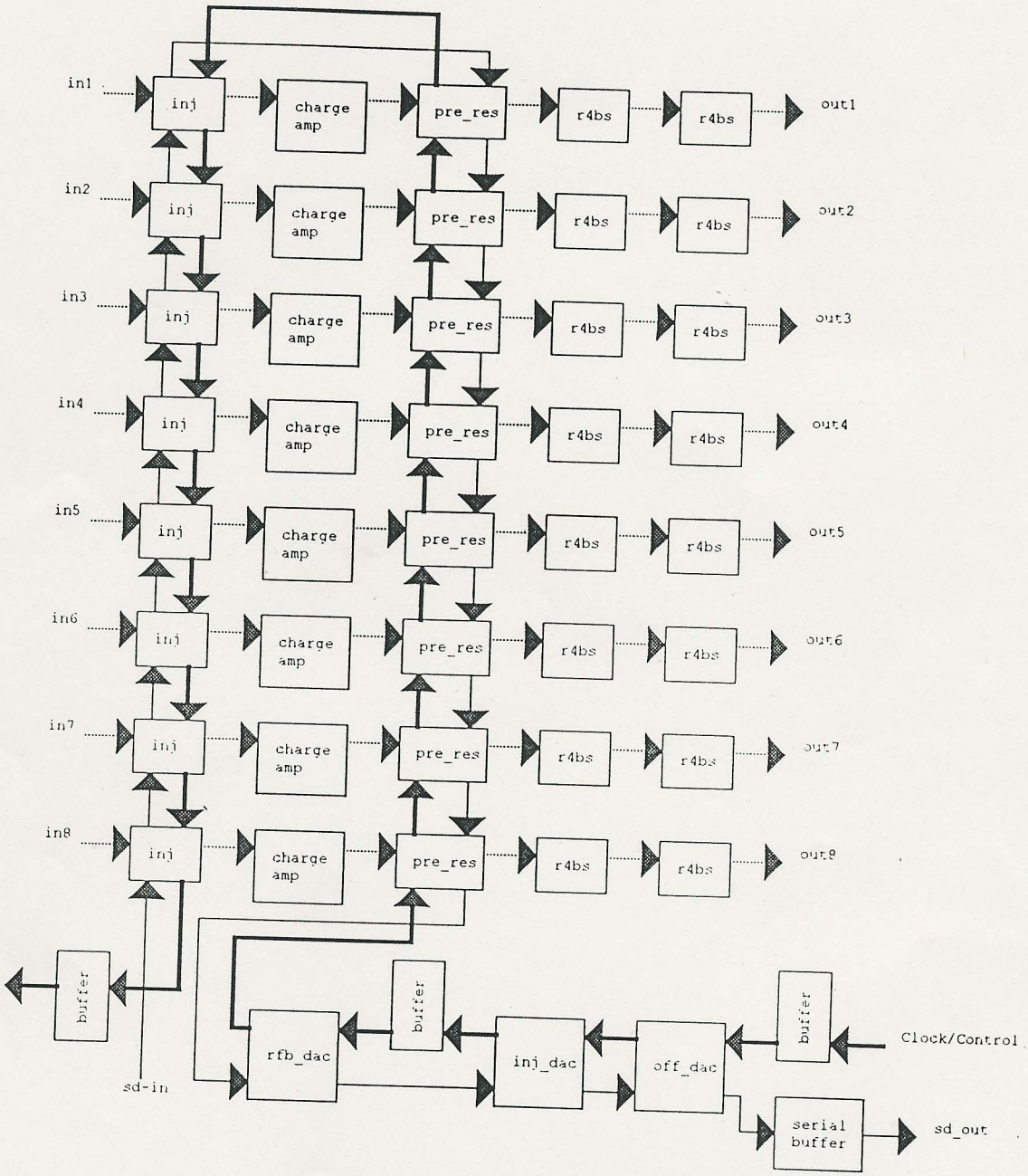

Figure 2. Serial data and clock signal flow.

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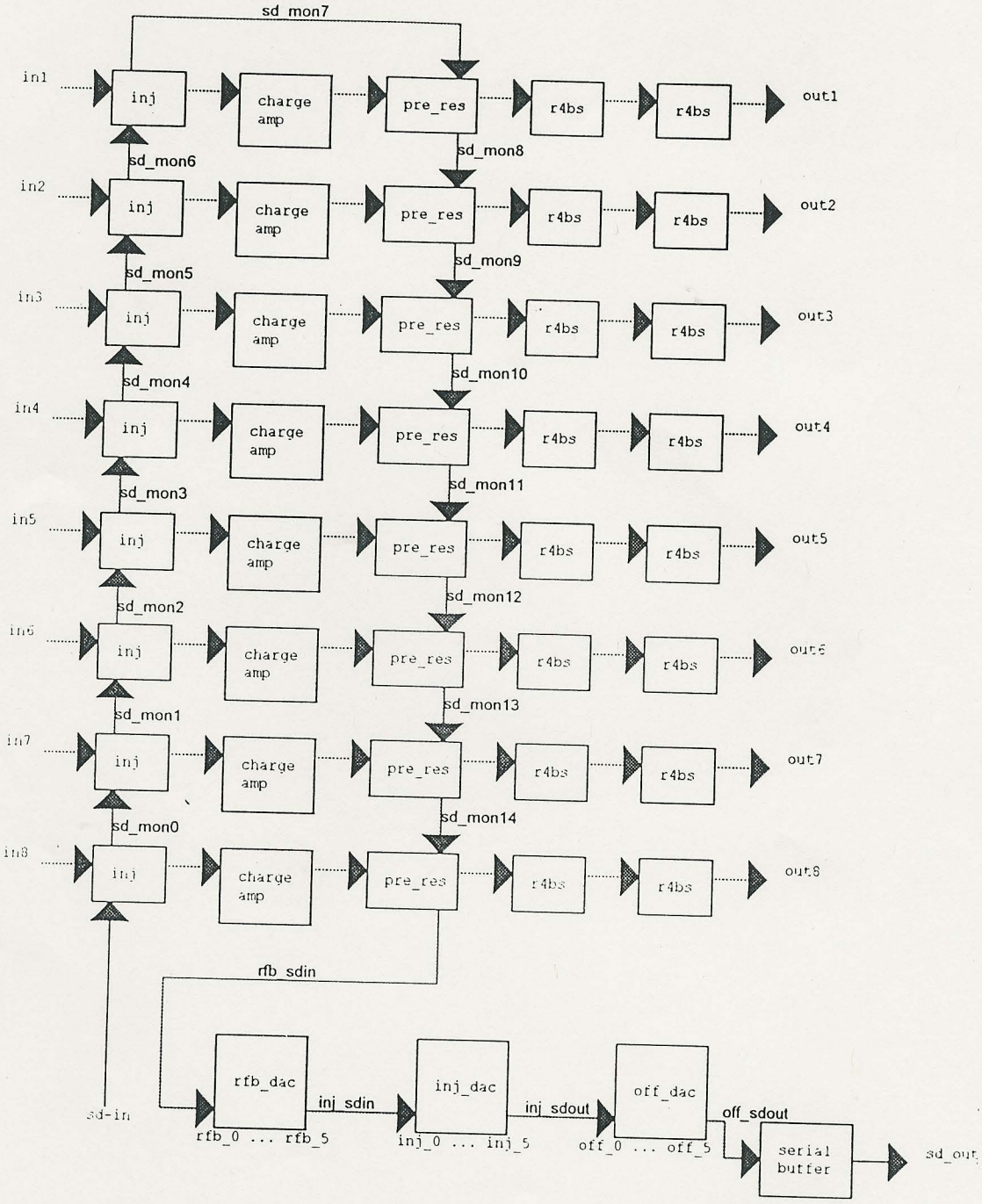

Figure 3. Serial data labels

7 PERFORMANCE

The expected performance of the CPA is listed below. The performance below assumes a detector capacitance of 10 – 200 pF.

Charge Sensitivity = ??

Noise referred to input ≤ 2000 e^- rms.
Channel – Channel gain matching = ??
Crosstalk to adjacent channel = ???
Peaking Time (C_{det} = 50 pF) = 900ns
(C_{det} = 200 pF) = 1100ns
Internal Test Pulse Capacitors = 260 fF

Output Impedance
Input impedance

Current consumption:
Idd-pre
Idd-shaper
Idd-dig
Power ≤ 50 mW / channel

Recommended Serial Clock Frequency = 1 MHz

Pedestal