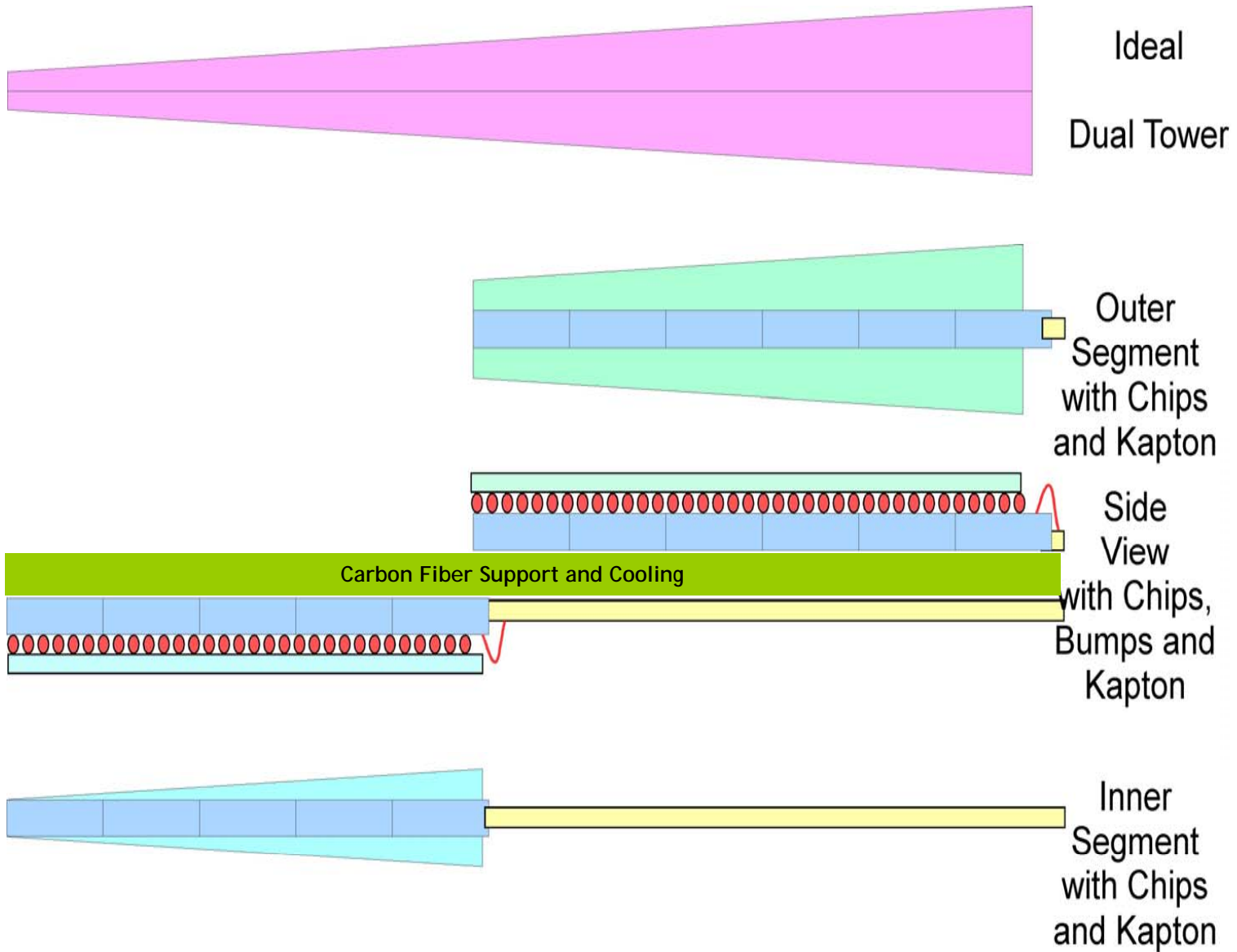
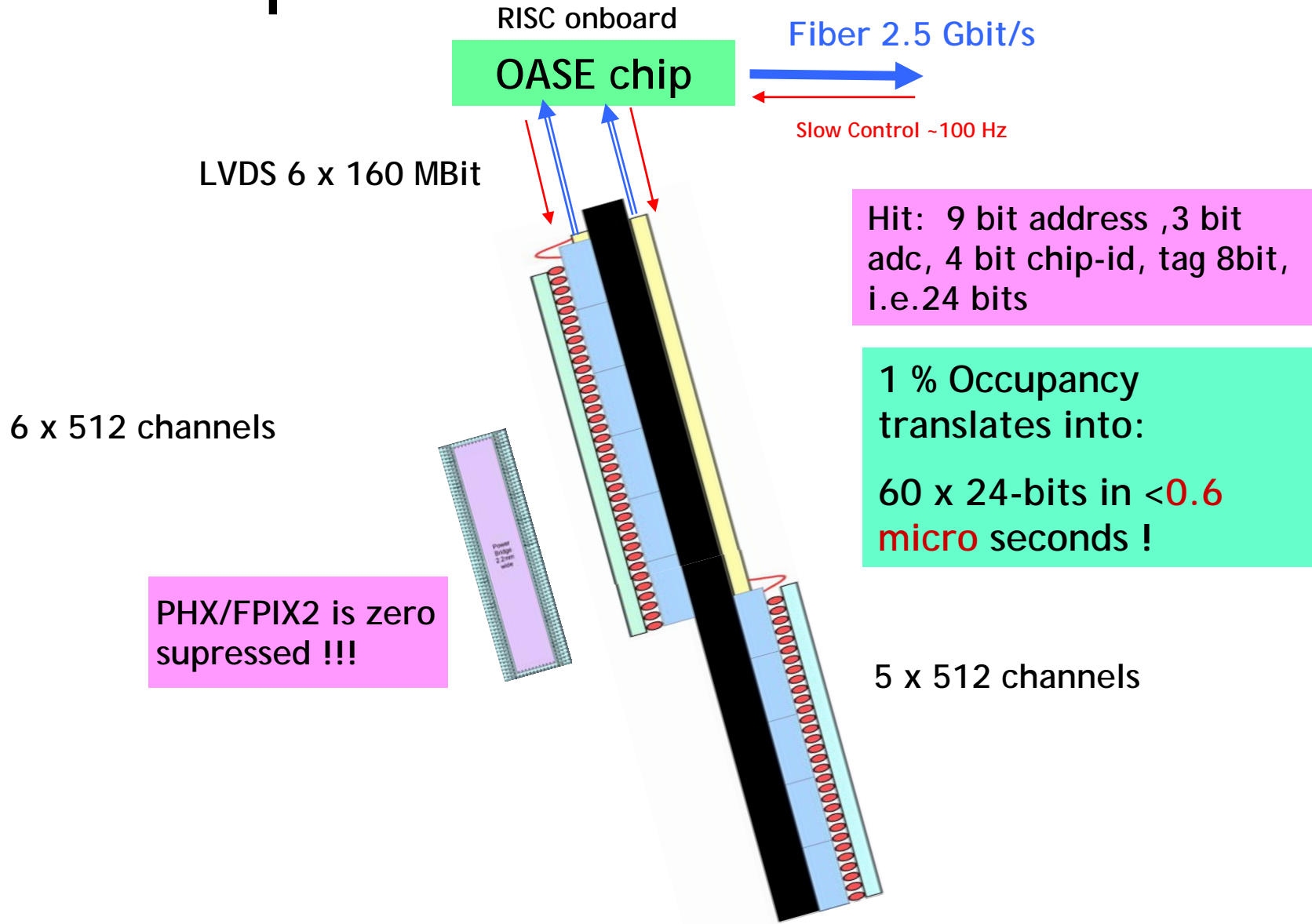


PHX: Tower Section



Endcap Readout: Front End



RISC onboard

OASE chip

Fiber 2.5 Gbit/s

Slow Control ~100 Hz

LVDS 6 x 160 MBit

Hit: 9 bit address, 3 bit adc, 4 bit chip-id, tag 8bit, i.e.24 bits

6 x 512 channels

1 % Occupancy translates into:
60 x 24-bits in <0.6 micro seconds !

PHX/FPIX2 is zero suppressed !!!

5 x 512 channels

Power Bridge 2 2pin wire

Endcap Readout: Back End

24 cards each end !

