SVX4 and PHENIX

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Proposed PHENIX sensor



- 3cm x 6cm device
- 80um × 1mm "pads" connected into 80um × 3cm strips
- 750 strips per orientation per sensor
- Readout at edges and center



- 128-channel Si-strip readout chip developed by FNAL/LBNL.
- Pipelined digitization and readout (42-deep pipeline for analog samples).
- 4-event LVL1-accept buffering.
- On-board zero-suppression available (or not).
- Multi-stage pedestal subtraction.
- Designed for AC-coupled device (Z. Li sensors DC-coupled). Two handles:
 - Frequent storage-cap resets.
 - Cool sensors to 0 degrees C to reduce leakage current.
 - Certainly able to do first. May suffice, but may want to cool anyway.
- Integration time (~80 ns) much shorter than sensors have been tested at. Possibly worse S/N.
- FNAL indicated willingness to do wafer-testing.



Where does SVX4 come in?



SVX4 Testboard



specify and download serial (mimics ARCNet) and mode-bit (mimics the GTM) control strings to the SVX4's on the hybrid through the input FIFO buffer. The mode-bit strings can contain L1 accepts and ENDDAT signals which will cause the SVX4 to dump data into the output FIFO buffer (mimics DCM) where they can be read by the PC.

Status

- Testboard in hand, populated, communication established.
- LabView GUI essentially finished.
- Testboard FPGA programming underway (estimate couple of weeks).
- Miljko goes on vacation for 1 month shortly, Vince to BNL (MuID) for 1 month shortly.
 - Hope to test compatibility w/ pseudo-PHENIX
 DAQ in August.
 - Test w/ sensor in September?