MVD Interface Module Testing - Hardware Configurations

MNE, MDA, MSE, GWT

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The interface modules associated with the MVD will require custom test hardware configurations for both initial unit functional tests and production unit checkout and qualification. Units addressed in this document include the DCM Interface Module (DCMIM), the Trigger Interface Module (TIM), and the Timing & Control Interface Module (TCIM). The testing requirements and associated test stand will be outlined for each of the individual modules, and a generic test stand that should meet the testing requirements of all three modules is described.

DCM Interface Module

The DCM interface module will reside in a 10U VME64X crate. A block diagram showing the interfaces to the unit is shown in Figure 1. The unit will consist of two physical cards -- a DCMIM Formatter Card and a Glink Transition Card. The two are connected using a VME backplane connector. Six MCM serial data busses (each consisting of 2 serial data channels for a total of 12 data channels) operating at ~40 Mbps deliver the MCM serial data packets to the DCMIM. Programming of the FPGAs is accomplished using the slow serial bus. Timing & Control signals are fed to the unit from the TCIM, and 6 Glink fibers carry formatted event data to the DCMs.

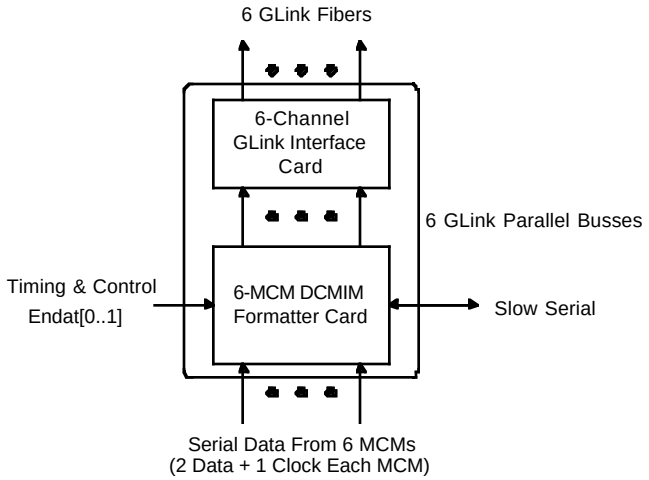

Figure 1. DCMIM Interfaces

For proper testing of the unit, each of these interfaces must be emulated using PC-based test hardware. Some functions such as the Glink fiber interface can be tested in pieces eliminating the need for 6 individual Glink receivers and data buffers.

The proposed test configuration is shown in Figure 2. The system is PC-controlled through the use of three CHZY (pronounced cheesy) cards. Fast signals (anything too fast for the PC to handle in real time) are managed using FIFOs. For this reason the Timing & Control Interface and the MCM Serial Data Interface (both output from the test stand) use a recirculating FIFO that allows full speed long term testing. Test sequences are loaded in a recirculating FIFO that allows the data to be looped and output indefinitely at PHENIX data rates. If there are difficulties meeting the speed requirements using this approach, a Lecroy arbitrary function generator can be used in place of the recirculating FIFO. However, this will make duplication of the test stand difficult. A Glink receiver and FIFO data buffer allow individual testing of the Glink interfaces. Multiples of this block can be added to the PCB making testing faster for the additional cost of Glink receivers. However, it is important to drive all MCM serial channels into the DCMIM to properly test the electronics as a system.

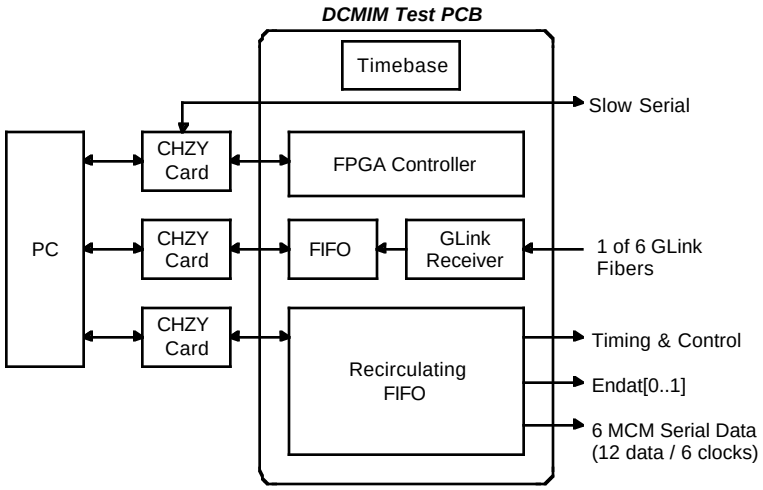

Figure 2. DCMIM Test Hardware Configuration (PC-Based)

Trigger Interface Module

The Trigger Interface Module (TIM) also resides in a VME crate (64x, 10U). Figure 3 shows the interrfaces associated with this unit. This unit will also consist of two physical cards -- a TIM functional card and an Interface Card. These two are also connected using a VME backplane connector. The exact partitioning of the module has yet to be finalized but certainly the Interface Card will include the Glink transmitters. The unit digitizes the trigger sums from 24 MCMs and transmits the data out the Glink Interface to the Global Trigger. Some subset of Timing & Control is required to properly test and operate the unit. -- namely the Beam Clock, FEM Reset, and possibly some mode bits for special command functions.

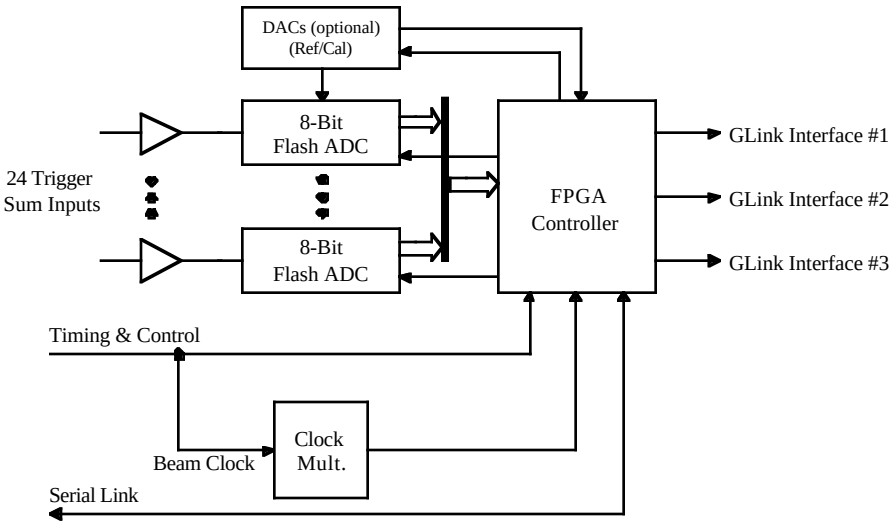

Figure 3. TIM Architecture and Interfaces

PC-based testing of the TIM requires the test configuration shown in Figure 4. This setup functions the same as the test stand for the DCMIM except that 24 analog trigger sums must be generated using DACs. The DACs will be programmed using the bits of the recirculating FIFO. Bits will be shared between DACs but uniquely configured so that each DAC has a unique analog output. The digitized and formatted trigger data transmitted by 3 Glink modules on the TIM will be input into the test PCB Glink receiver and stacked in a FIFO for later retreival by the PC. A deep FIFO will be used here so that test runs can be as

long as possible. Following a test, the PC will retreive the data from the FIFO and check the formatted results.

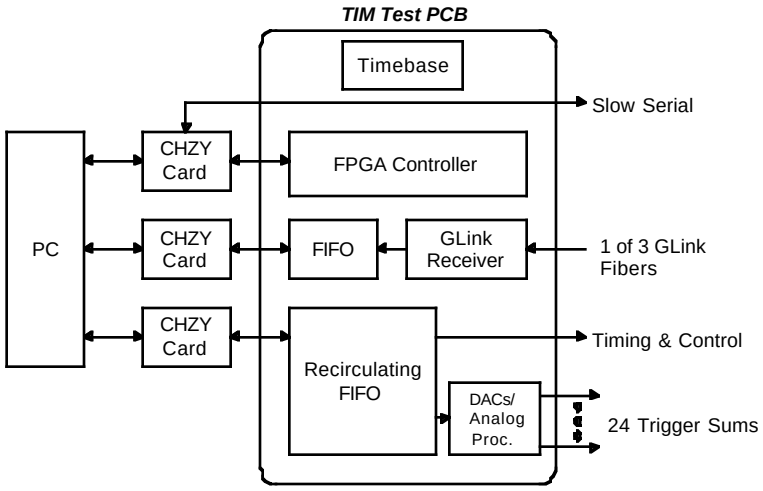

Figure 4. TIM Test Hardware Configuration (PC-Based)

Timing & Control Interface Module

The Timing & Control Interface module will also reside in a 10U VME crate and will have an associated transition module. A diagram showing the basic functional blocks and associated interfaces is shown in Figure 5. The timing input to the module is received on a Glink fiber and is fanned out and redistributed to 14 MCM group busses and the VME backplane. Each MCM bus consists of 6 MCMs, all residing on the same MCM interconnection cable or board. The timing distributed to the VME backplane is for use by the other interface modules residing in the same crate. The ARCNet controller provides slow serial busses to the 14 MCM groups and to the VME backplane.

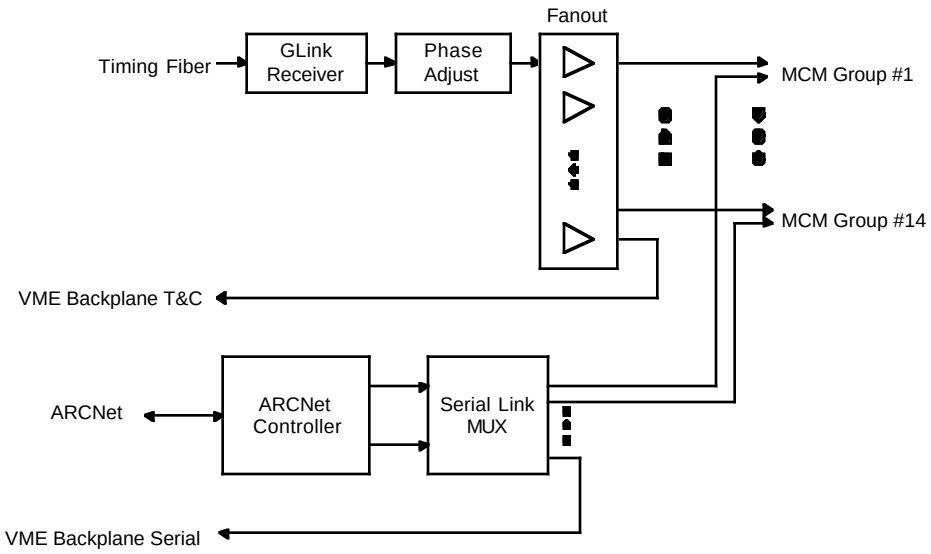

Figure 5. TCIM Unit and Interfaces

The hardware requirements for testing the TCIM are shown in Figure 6. The timing fiber signal is generated using a recirculating FIFO and Glink transmitter. The timing and control fanout (including

timing and slow serial) that is sent to both the MCM group busses and the VME backplane will be plugged into the Test PCB (one group at a time) and stored in a FIFO for post-test data retreival and comparison. This will varify proper operation of both the Glink interface, fanout, and ARCNet functions. Timing specifics (phase adjust, overshoot, phase matching between channels, noise, etc.) will be evaluated by incremental loading of the busses with the appropriate cables, PCBs, and test loads (motherboard, MCM bus cabling, etc.). This will have to be observed and evaluated using an oscilloscope.

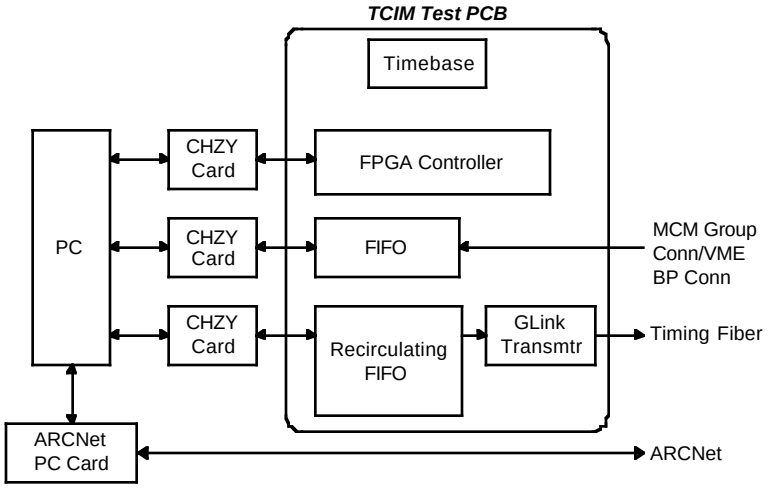

Figure 6. TCIM Test Hardware Configuration (PC-Based)

Generic Test Hardware

Comparison of the hardware test needs of each of the interface modules shows that a generic system can be developed that will meet all the interfacing and test needs of the three interface modules (see Figures 2, 4, and 6). The block diagram for this system is shown below. Separate software routines (written using LabView) will exist for testing each type of interface module. With all the interfaces that exist, the unit can also easily be adapted for MCM checkout.

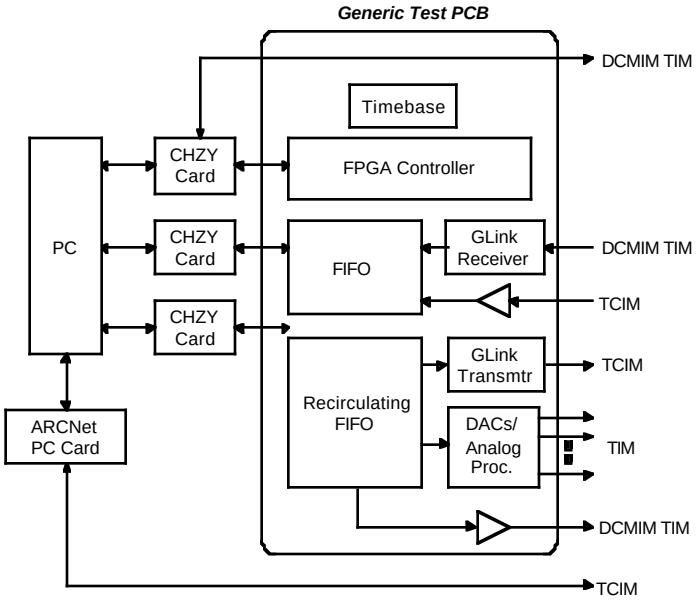

Figure 7. Generic Interface Module Test System