Test Vector Generation for the MVD AMUADC and TGV32

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Section 1. AMUADC Test Specifications

by Mike Emery
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OVERVIEW

A description of test requirements and specifications needed for known-good-die wafer probing of the AMU-ADC chip is described in this document. The chip is a 32 channel CMOS analog memory and 12 bit analog to digital converter. Each channel of analog memory contains 64 cell addresses. An analog signal is sampled by the AMU and written into a specific address by the WRITE address bus and Write Enable signal. Reading the contents of the analog memory is controlled by the READ address bus and the Read Enable signal. There are three digital to analog converters to provide analog references needed by the AMU and the ADC. Two of the DACs are voltage output, and the third is current output. The clock needed by the ADC is differential positive emitter coupled logic level (PECL). An output data register is provided on-chip to hold one conversion-worth of data so that "pipeline" operation is possible; i.e. performing a new conversion at the same time that the previous conversion is being read out.

The pin-out of the AMUADC is shown in Table 1. The list begins at the lower left-hand corner of the die and proceeds counter-clockwise around the chip. (Pin 1 is defined in the middle of the east side of the die.)

Table 1. Identification and function of AMUADC bonding pads.

IC Pad No.	Name	Description
82	AGND	Analog Ground. SW Corner.
83	MUX1_OUT	Output for monitoring AMU at input. Requires channel address from serial data string.
84	CORR_OFF_DAC	DAC output to supply CORR_OFF_IN.
85	CORR_OFF_IN	Correlator Offset Input.
86	MUX2_OUT	Output for monitoring AMU at output. Requires channel address from serial data string.
87	IREF_DAC	DAC current output to supply IREF_IN.
88	IREF_IN	Sets slew rate for ADC Ramp Generator.
89	IBIAS_RAMP	Bias current for Ramp Generator circuit. Internal biasing provided, but may be modified externally with resistor network.
90	VREF_DAC	DAC output to supply VREF_IN.
91	VREF_IN	Reference Voltage for ADC. Sets the starting voltage of the ADC Ramp. Vref ≤ 4.8V
92	AVDD7	Analog VDD. Typical Vdd = 5V.
93	AGND7	Analog Ground.
94	DAC_AMP_BIAS	Bias monitor pin for DAC bias. (Output, hi Z)
95	DAC_VMID	Input reference voltage. Typical = Vdd / 2
96	NC	Ground to most convenient ground.
97	IREF_BIAS	Bias for DAC used for IREF. Internal biasing provided, but may be modified externally with resistor network.
98	AGND4	Analog Ground. Comparator. Same as i.c. pad number 23. Both connections are needed.
99	AVDD4	Analog VDD. Typical Vdd = 5V. Comparator. Same as i.c. pad number 22. Both connections are needed.
100	DVDD3	Digital Vdd. Typical Vdd = 5V.
101	DGND3	Digital Ground
102	SD_IN	Serial Data input
103	SR_RST	Serial Data reset input. Active HIGH.

104	WREN	AMU Write Enable input. Active HIGH.
105	WR0	AMU Write Address 0
106	WR1	AMU Write Address 1
107	WR2	AMU Write Address 2
108	WR3	AMU Write Address 3
109	WR4	AMU Write Address 4
110	WR5	AMU Write Address 5
111	DCLK_IN	Latches serial data. Rising edge. Input.
112	RDBK_IN	Readout latched serial data for verification. Input. Logic 1 - Readback; Logic 0 - input. See Serial Data String documentation for proper protocol.
113	SHFT_CLK_IN	Shift register clock input for Serial Data input. Typical frequency 1 MHz. Rising Edge. See Serial Data String documentation for proper protocol.
114	SD_OUT	Serial Data Out.
115	SLCT1	ADC Mode Conversion bit 1. 00 = 9 bit, 01 = 10 bit, 10 = 11 bit, and 11 = 12 bit ADC conversions (SLCT1, SLCT0). Input.
116	SLCT0	ADC Mode Conversion bit 0. 00 = 9 bit, 01 = 10 bit, 10 = 11 bit, and 11 = 12 bit ADC conversions. Input.
117	IBIAS_CLK	Bias for ADC high-speed PECL-CMOS clock circuit. Intermal biasing provided suitable for low-speed operation, but may be modified externally with resistor network. For high-speed operation connect resistor (typically 40KΩ) between VDD (digital) and IBIAS_CLK.
118	ADC_CLK_EN	ADC Clock Enable input. Assert high. Starts a conversion by starting the Ramp Generator and Counter simultaneously. Remains high until FSC. (ADC_CLK_EN resets adc counter when low.)
119	DVDD	Digital VDD. Typical Vdd = 5V. SE Corner.
120	ADC_CLK+	High speed clock input for ADC. Requires 50% duty cycle, PECL logic levels. Maximum frequency ≈ 210 MHz. Complement of ADC_CLK−.
121	ADC_CLK−	High speed clock input for ADC. Requires 50% duty cycle, PECL logic levels. Maximum frequency ≈ 210 MHz. Complement of ADC_CLK+.
122	FSC	Full Scale Count. This output indicates (active High) that an ADC conversion is complete. Data is now ready for loading and read out.
123	ADC_A4	ADC channel address 4.
124	ADC_A3	ADC channel address 3.
125	ADC_A2	ADC channel address 2.
126	ADC_A1	ADC channel address 1.
127	ADC_A0	ADC channel address 0.
128	ADC_OE	ADC Output Enable. Output is High Z when ADC_OE is low.
129	DGND2	Digital Ground.
130	DVDD2	Digital Vdd. Typical Vdd = 5V.
131	ADC_OUT0	ADC Output bit 0. (LSB)
1	ADC_OUT1	ADC Output bit 1.
2	ADC_OUT2	ADC Output bit 2.
3	ADC_OUT3	ADC Output bit 3.
4	ADC_OUT4	ADC Output bit 4.
5	ADC_OUT5	ADC Output bit 5.
6	ADC_OUT6	ADC Output bit 6.
7	ADC_OUT7	ADC Output bit 7.
8	ADC_OUT8	ADC Output bit 8.
9	ADC_OUT9	ADC Output bit 9.
10	ADC_OUT10	ADC Output bit 10.

11	ADC_OUT11	ADC Output bit 11. (MSB)
12	DGND	Digital Ground. NE Corner.
13	DGND1	Digital Ground
14	DVDD1	Digital Vdd. Typical Vdd = 5V.
15	ADC_LOAD	Input. Load ADC Data into latch. Assert high.
16	DB_RST	Input. ADC Debounce Reset. Reset debounce circuits. Assert high.
17	COMP_RST	Input. ADC Comparator Reset. Assert high.
18	AZ	Input. ADC Auto-Zero. Assert high.
19	ICS	Input. ADC Internal Comparator Switch. ICS=0 looks at analog input signal; ICS=1 looks at RAMP.
20	FRAMEBREAK	Ground to most convenient ground.
21	RAMP_OUT	ADC RAMP output signal. Starts high (at VREF) and slews negative toward 0V.
22	AVDD3	Analog Vdd. Typical Vdd = 5V. Comparator. Same as i.c. pad number 99. Both connections are needed.
23	AGND3	Analog Ground. Comparator. Same as i.c. pad number 98. Both connections are needed.
24	AGND6	Analog Ground.
25	AVDD6	Analog Vdd. Typical Vdd = 5V.
26	VMID2	Input reference voltage. Typical = Vdd / 2
27	FRAMEBREAK	Ground to most convenient ground.
28	CORR_BIAS	Bias current for Correlator circuit. Intermal biasing provided, but may be modified externally with resistor network.
29	CORR_RST	Correlator Reset input for AMU Correlator circuit. Assert high.
30	AMP_RST	Reset input for AMU readout buffer amplifier. Assert high.
31	CONN	Connects AMU output to ADC (or Correlator). Input. Assert high.
32	RD5	AMU Read Address 5.
33	RD4	AMU Read Address 4.
34	RD3	AMU Read Address 3.
35	RD2	AMU Read Address 2.
36	RD1	AMU Read Address 1.
37	RD0	AMU Read Address 0.
38	RD_EN	Read Enable input for AMU. Assert high.
39	DGND4	Digital Ground.
40	DVDD4	Digital Vdd. Typical Vdd = 5V.
41	FRAMEBREAK	Ground to most convenient ground.
42	AGND2	Analog Ground.
43	AVDD2	Analog Vdd. Typical Vdd = 5V.
44	VMID	Input reference voltage. Typical = Vdd / 2
45	AVDD	Analog Vdd. Typical Vdd = 5V. NW Corner
46	AVDD1	Analog Vdd. Typical Vdd = 5V.
47	AGND1	Analog Ground.
48	IN0	Input channel 0
49	IN1	Input channel 1
50	IN2	Input channel 2
51	IN3	Input channel 3
52	IN4	Input channel 4
53	IN5	Input channel 5
54	IN6	Input channel 6
55	IN7	Input channel 7
56	IN8	Input channel 8
57	IN9	Input channel 9
58	IN10	Input channel 10
59	IN11	Input channel 11

60	IN12	Input channel 12
61	IN13	Input channel 13
62	IN14	Input channel 14
63	IN15	Input channel 15
64	IN16	Input channel 16
65	IN17	Input channel 17
66	IN18	Input channel 18
67	IN19	Input channel 19
68	IN20	Input channel 20
69	IN21	Input channel 21
70	IN22	Input channel 22
71	IN23	Input channel 23
72	IN24	Input channel 24
73	IN25	Input channel 25
74	IN26	Input channel 26
75	IN27	Input channel 27
76	IN28	Input channel 28
77	IN29	Input channel 29
78	IN30	Input channel 30
79	IN31	Input channel 31
80	AGND5	Analog Ground.
81	AVDD5	Analog Vdd. Typical Vdd = 5V.

Whenever a die fails a test, no further testing is necessary and the die may be marked as bad. Testing may then proceed to the next die.

I. QUIESCENT CURRENT

All control signals are at 0 volts.
Supply 2.5 Vdc reference to the following pads: 26, 44, 95
Supply 5 Vdc power to the Vdd pads below.
Supply 0 Vdc power (ground) to the GND pads below.
Measure the following power supply currents shown in Table 2:

Table 2. Power pads and performance.

PAD	FUNCTION	CURRENT
22+99	Comparator Vdd	.1mA maximum
23+98	Return for Comparator Vdd	
25+43+45+46+81+92	Analog Vdd	0.4 mA maximum
24+42+47+80+82+93	Return for Analog Vdd	
14+40+100+119+130	Digital Vdd	0.2 mA maximum
12+13+39+101+129	Return for Digital Vdd	

If the measured current exceeds the values specified in the table above the die fails and should be marked as bad. Also, a “zero” reading on any of the Analog power or ground pads indicate failure. Zero on digital or Comparator lines does <u>not</u> indicate failure (at this time).

Apply a logic “1”, 5 Volt, to the AZ line, pad 18. Measure the supply current at the following pads indicated in Table 3, then return AZ to logic “0” when measurement is complete:

Table 3. Power performance with AZ high.

PAD	FUNCTION	CURRENT
22+99	Comparator Vdd	24 mA, ±25%
23+98	Return for Comparator Vdd	

If the measured current falls outside this window, the die fails. Also, if one pad draws less than 20% of the total current, the die fails.

The power will be maintained for the remainder of the tests until the die either fails or passes.

II. SERIAL COMMUNICATIONS

The AMUADC must be configured with a 33 bit long serial data string. This data controls the DAC values, sets up input and output "spy" multiplexers for monitoring the AMU operation, and sets the Correlator Select bit. Serial communication protocol is identical to the TGV32 chip. Bit definition is described in Table 4.

Table 4. List of Serial Data String, listed in order of first-in to last-in.

Bit #	Label	Function	Bit #	Label	Function
1	MUX2_OE	Mux 2 Output Enable	18	DAC2_4	DAC V_{CORR} Code bit 4
2	MUX2_0	Mux 2 Address LSB	19	DAC2_5	DAC V_{CORR} Code bit 5
3	MUX2_1	Mux 2 Address bit 1	20	DAC1_0	DAC I_{REF} Code bit 0
4	MUX2_2	Mux 2 Address bit 2	21	DAC1_1	DAC I_{REF} Code bit 1
5	MUX2_3	Mux 2 Address bit 3	22	DAC1_2	DAC I_{REF} Code bit 2
6	MUX2_4	Mux 2 Address bit 4	23	DAC1_3	DAC I_{REF} Code bit 3
7	CORR_SEL	Correlator Select control bit	24	DAC1_4	DAC I_{REF} Code bit 4
8	DAC3_0	DAC V_{REF} Code bit 0	25	DAC1_5	DAC I_{REF} Code bit 5
9	DAC3_1	DAC V_{REF} Code bit 1	26	MUX2-HIZ	Mux 2 pull-down
10	DAC3_2	DAC V_{REF} Code bit 2	27	MUX1-HIZ	Mux 1 pull-down
11	DAC3_3	DAC V_{REF} Code bit 3	28	MUX1_OE	Mux 1 Output Enable
12	DAC3_4	DAC V_{REF} Code bit 4	29	MUX1_0	Mux 1 Address LSB
13	DAC3_5	DAC V_{REF} Code bit 5	30	MUX1_1	Mux 1 Address bit 1
14	DAC2_0	DAC V_{CORR} Code bit 0	31	MUX1_2	Mux 1 Address bit 2
15	DAC2_1	DAC V_{CORR} Code bit 1	32	MUX1_3	Mux 1 Address bit 3
16	DAC2_2	DAC V_{CORR} Code bit 2	33	MUX1_4	Mux 1 Address bit 4
17	DAC2_3	DAC V_{CORR} Code bit 3			

Data is shifted in and latched on the rising edge of the shift clock and data clock lines respectively. Data setup time is 100 ns, hold time is 20 ns. Logic levels are standard 5 volt CMOS. The shift clock frequency will be 1 MHz nominally, pulses will be positive-going with a duration between 90 to 110 ns.

The communications test will consist of resetting the chip by sending a 100 ns pulse to Serial Reset, then reading the chip configuration and verifying the following pattern (expressed in hexadecimal):
`00000000(hex)`

Next write, latch, readback and verify the following pattern:
`0AAAAAAA (hex)`

Next write, latch, readback and verify the following pattern:
`15555555 (hex)`

Reset chip. This completes the communications test. The die fails if the data readback does not conform to this test.

III. DAC AND BIAS VOLTAGES

There are three 6-bit DACs on this chip. Two are voltage output, and the third is current output. The V_{REF} DAC is designed for rail-to-rail output, 0 - 5 Vdc. The V_{CORR} DAC has an output range of 0 - 2.5 Vdc. The I_{REF} DAC has an output range of 0 - 75 uA.

Measure the voltage at the following pads shown in Table 5 to verify proper DAC biasing:

Table 5. DAC bias voltages.

Pad	Function	Volts
94	DAC_AMP_BIAS	3.7 ± 20%
97	IREF_BIAS	3.7 ± 20%

Using the serial communication protocol described above, load the following DAC codes and measure the DAC outputs as shown in Table 6. The DAC codes are in the following order: Bit 5 (MSB) - Bit 0 (LSB).

Table 6. DAC binary test codes and expected output (± 20%).

V_{REF}	V_{CORR}	I_{REF}	V_{REF} Out (dc Volt)	V_{CORR} Out (dc Volt)	I_{REF} Out (dc μA)
000000	000000	000000	<0.4	<0.15	>70.0
000001	000001	000001	0.4	0.16	71.3
000010	000010	000010	0.48	0.20	70.2
000100	000100	000100	0.63	0.27	67.7
001000	001000	001000	0.93	0.42	63.0
010000	010000	010000	1.56	0.74	53.8
100000	100000	100000	2.73	1.30	35.9
111111	100000	100000	4.80	1.30	35.9
100000	111111	100000	2.73	2.50	35.9
100000	100000	111111	2.73	1.30	<2.0

The die fails if the measured voltages and currents fall outside the specified tolerances.

IV. ADC COUNTER

The counter on the ADC section of the AMUADC counts both edges of a differential positive emitter-coupled-logic level clock to either 9, 10, 11, or 12 bits depending on the SLCT1 and SLCT0 pins. When the counter has reached the end of its counting range a Full Scale Count, FSC, flag is set true. This is the indication that a conversion cycle is complete. The time t_{conv} required between starting the counter (Clock Enable starts the sequence) and FSC going true is given by the equation

$$t_{conv} = \frac{2^{n-1}}{f_{ADC}},$$

where n is the number of bits being counted, and f_{ADC} is the differential clock frequency. Synchronizing circuitry adds another 2-5 clock periods.

Provide a 50% duty cycle differential positive emitter coupled logic (PECL) level clock running at a frequency of 40 MHz to pads 120 and 121. Set the two mode-select pads, 115 and 116, high. This places the ADC in 12-bit counting mode. Assert the Clock Enable, pad 118, high and observe when FSC, pad 122, goes high. FSC should go high between 51.2 μs and 51.4 μs after Clock Enable starts. Step

through each combination of SLCT0 and SLCT1 and measure the time to FSC. Results should agree with Table 7 below.

Table 7. ADC counter modes and FSC times for a 40 MHz ADC clock.

Mode	SLCT1	SLCT0	FSC: t_{conv} (μs)
9-bit	0	0	6.4 ↔ 6.6
10-bit	0	1	12.8 ↔ 13.0
11-bit	1	0	25.6 ↔ 25.8
12-bit	1	1	51.2 ↔ 51.4

The die fails if FSC does not occur, if t_{conv} does not halve with each step from 12-bit to 9-bit, or if t_{conv} falls outside of specifications.

V. Testing for Stuck At One Bits

Place chip in 12 bit mode. Disable ADC Clock. Cycle Clock Enable high and back low. Cycle the LOAD pad 15 high and back low. Set Output Enable pad 128 high and read out all 32 channels. Channel address bus is pads 127 (LSB), 126, 125, & 124 (MSB). The data output pads are 131 (LSB), 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, & 11 (MSB). All data bits should be logic '0' in all 32 channels. If any data bits are logic '1' the die fails. (Stuck at '0' test will be performed in a later step.)

VI. Ramp Generator Circuit

Connect the VREF_DAC to VREF_IN (pads 90 and 91), and IREF_DAC to IREF_IN (pads 87 and 88).

Measure the dc voltage at IBIAS_RAMP pad 89. The voltage should be 0.86 Volt ± 25%.

Set Clock Enable pad 118 low.

Load V_{REF} DAC serial register with 100000 (binary). Measure the dc voltage of the V_{REF} DAC output pad 90 and of the RAMP_OUT pad 21. Each should measure 2.7 Volt ± 25%. Calculate the voltage difference between VREF_DAC and RAMP_OUT. The difference should be less than ± 50 mV. The die fails if the voltage difference is greater than ± 50 mV.

Load V_{REF} serial register with 111000. V_{REF} should measure 4.5 V ± 25%.

Load I_{REF} serial register with 011111. I_{REF} should measure 36.7 μA ± 25%.

Assert Clock Enable pad 118 high. A negative-going linear voltage ramp should be observed on RAMP_OUT pad 21. The ramp voltage should start at V_{REF} and slew toward 0 volts, where it will end. Measure the slew rate. The slew rate should be 1.3 Volt/μs ± 30%. Return Clock Enable to logic '0' and verify that RAMP_OUT resets to its original voltage in less than 2 μs. The die fails if the ramp fails to occur, if the slew rate falls outside of specifications, or fails to reset.

MEMORY CELL SCAN AND DATA READOUT

The remaining sequence of tests will operate the chip as an entire system. This is necessary to validate the analog memory and the ADC. To run the entire chip several things have to happen in the proper sequence. These will discussed one at a time below.

WRITING TO THE AMU

Each of the 64 memory cells in each of the 32 pipes must be tested and verified. Verification will require storing and reading a low voltage less than 1 volt, a mid-range voltage around 2.5 V, and a high voltage around 4 V. First, data must be written into the memory by placing an analog dc voltage to all 32 inputs. The writing to the AMU is done by placing the desired address on the WRITE address bus and then clocking the Write Enable. Write Enable should be high a minimum of 50 ns. If a 50% duty cycle is used the maximum frequency for Write Enable would be 10 MHz. Figure 1 shows the writing protocol. The address lines must be settled before Write Enable begins.

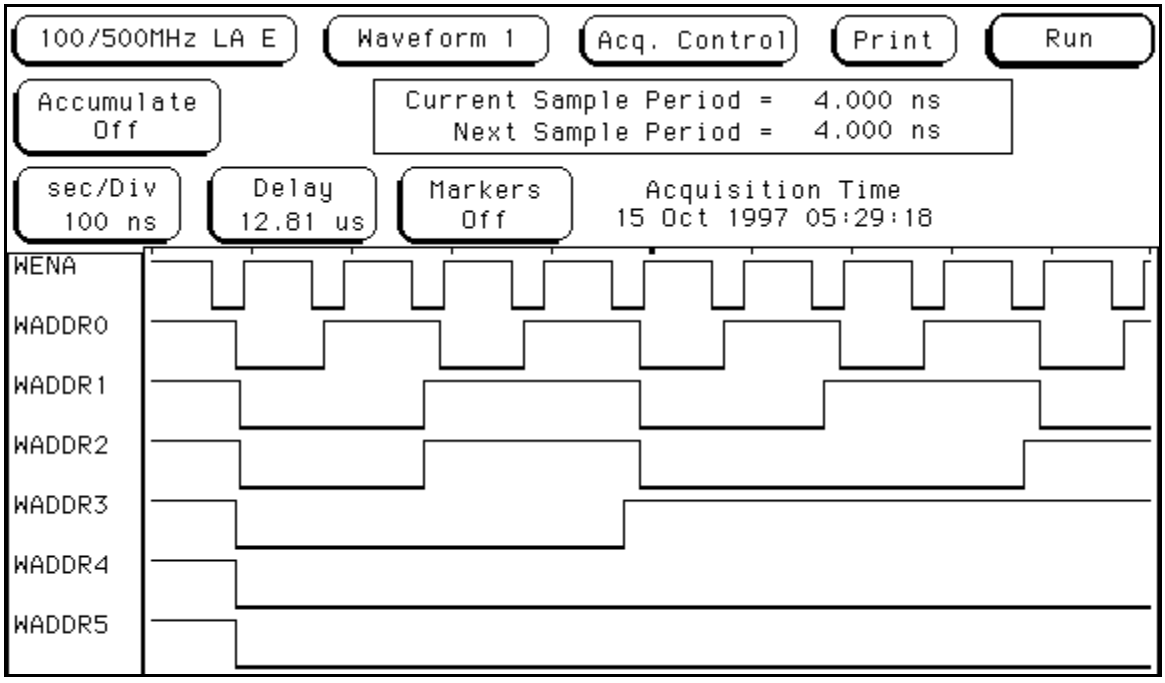


Figure 1. Writing to the analog memory.

READOUT OF AMU AND ADC SETUP

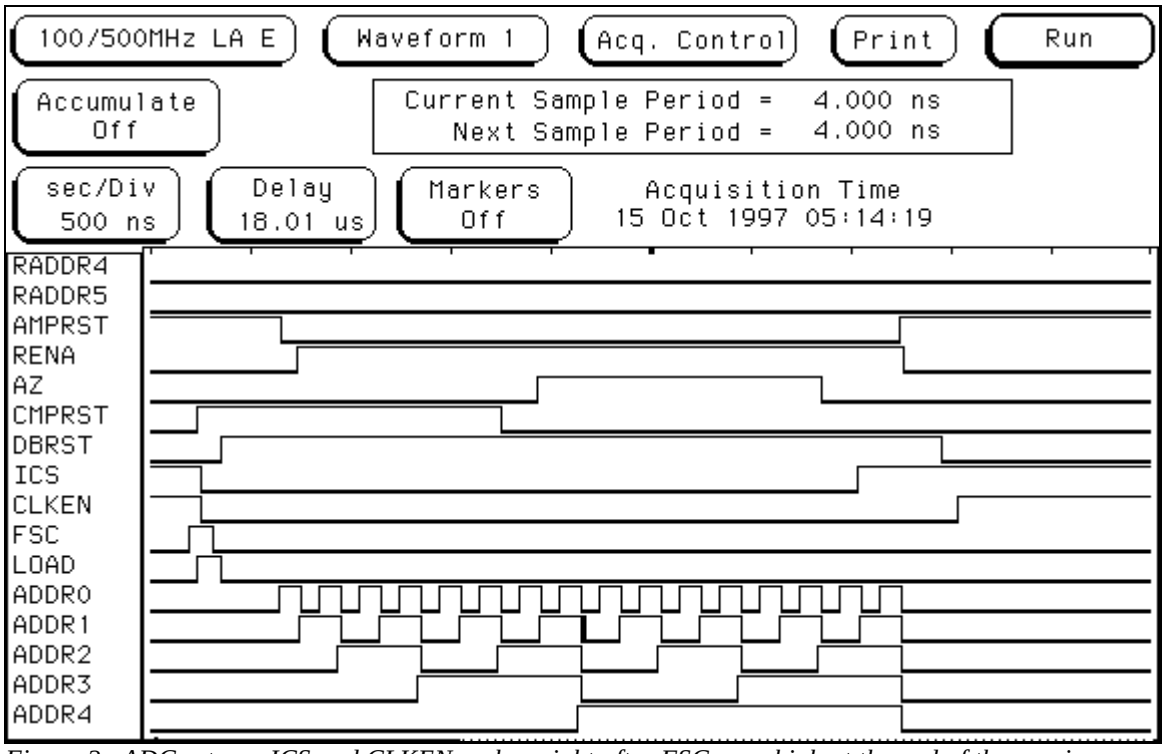


Figure 2. ADC set up. ICS and CLKEN go low right after FSC goes high at the end of the previous conversion. The LOAD and data output address lines are cycled through during the setup for the next conversion.

Readout of the AMU and digitizing the value is done by placing the desired cell address on the Read Address bus, setting the Read Enable high and setting up the ADC and running a conversion. The digitized data is then read out of all 32 channels. The values will probably not be identical from one channel to another, but should agree within about ± 100 counts. The low voltage test should produce results below about 1000, the midrange test should result in data around 2000, and the high voltage test should produce results greater than 3000 but less than 4095. Figure 2 shows the ADC setup and conversion process.

The ramp generator must be set up correctly. As described above, the ramp signal starts at VREF and slews negative toward ground. Proper setup will have the ramp reaching ground at about the same time the FSC occurs. Figure 3 shows a typical adjustment of the ramp. Ground reference for each displayed signal is indicated by the arrows on the left-hand side of the graph. The needed slew rate depends on the ADC clock speed and the number of bits being counted. Due to fabrication variations the actual values needed by the VREF_DAC and the IREF_DAC in order to obtain an optimum

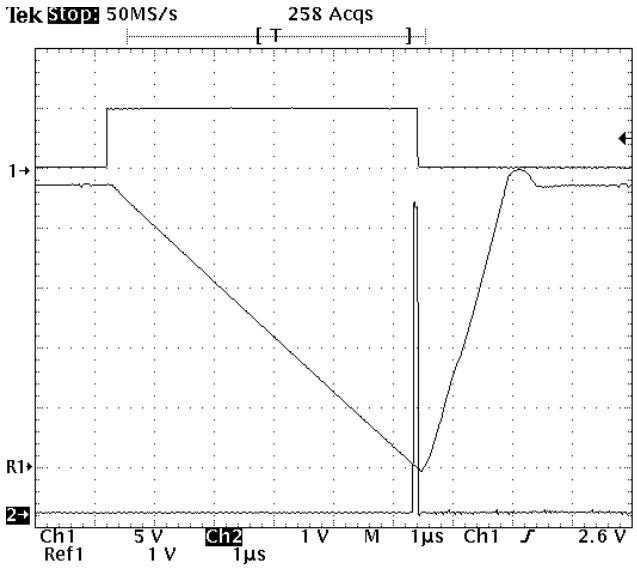


Figure 3. Typical ramp signal. Top trace is Clock Enable, middle trace is the ramp, bottom trace is FSC.

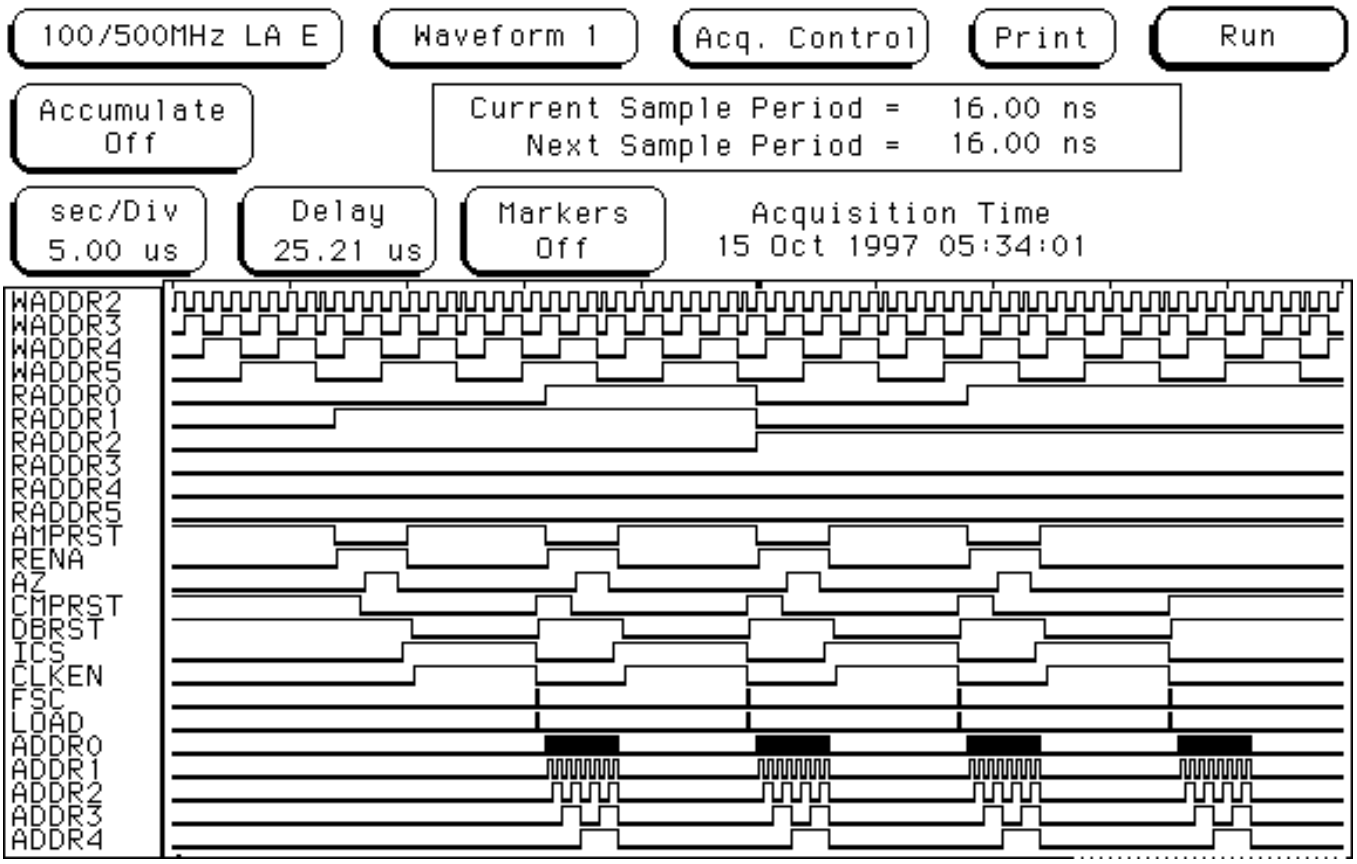


Figure 4. Four rapid conversions.

setup may differ slightly from the following setup

The needed settings for these tests should be 12-bit mode, ADC clock frequency set at 40 MHz, so FSC should occur 51.2 μs after Clock Enable. The DAC value for VREF DAC is 55 or approximately 4.5 volt, the DAC value for the IREF DAC should be 60 to produce a ramp slew rate of 0.086 V/μs ± 20%. It is important to keep in mind that the purpose of this test is not to calibrate but to verify. Therefore as long as the ramp has a linear shape and falls below the low-voltage input before FSC occurs the results will be meaningful. If the ramp does not get below the low-voltage signal, the comparators will not fire and the result will be 4095 and consequently not give any information about the memory cell.

Figure 4 shows several conversions taking place in rapid succession. This is provided to help make the above sequences more clear. All of these operations have to play together at the same time and in the right order.

VII. Stuck at Zero Test

As a final test to check for stuck at zero bits, an input voltage of 5 volts should be loaded into memory and converted. All digitized results should be 4095. Any other values cause the die to fail.

VIII. AMU Cell Verification

Each of the 64 memory cells in each of the 32 pipes must be tested and verified. Load the entire AMU first with a 0.9 volt level, then repeat the test with a mid-range 2.5 V, and repeat the test with a high voltage 4.0 V signal.

Readout all cells in all pipes for each of the three input voltages. The low level test should result in digitized results below 1000 (decimal) for all cells. The 2.5 V test should result in digitized results from 1500 – 2500 (decimal). The 4.0 V test should result in all cells reading out over 3000 (decimal) but less than 4095. Store these values for later calculation of pedestal offsets.

The chip passes this test if all 2048 memory cells (64 cells/pipe by 32 pipes) successfully convert all three voltage inputs.

Calculate pedestal offset for each of the three previous tests as follows: calculate the average value for each of the 32 pipes. Subtract the average value for the pipe from the value for each cell in that pipe. The absolute value of the difference should be less than 30 (decimal) for each cell. If the pedestal offset exceeds the specification the die fails.

IX. CORRELATOR MODE

The last remaining test requires making a couple more conversions, this time using the correlator. A step input voltage must be provided such that the step occurs between two predetermined cell write addresses. This mode uses a correlator circuit to measure the difference between the two cells during the readout operation. The correlator circuit is enabled by setting the CORR_SEL bit high in the serial data string. Figure 5 shows the proper timing signals to operate with the correlator circuit. Note that the CONN signal goes low (disconnecting) at appropriate times.

The Correlator DAC should be loaded with (binary) 100000 (about 1.3 volt output). This is an offset voltage used by the correlator. The voltage difference that exists between the two cell addresses is added to the correlator offset voltage, and the total voltage is then digitized. If no voltage difference exists only the correlator offset is digitized.

The pulse should step from 2 V to 3 V with a risetime less than 100 ns. Cell addresses 20 and 30 may be used as the correlated cell addresses. The transition should occur at a time between writing to cell addresses 20 and 30.

First, make a correlator-mode conversion with no pulse. Read out all channels. The value should be around 1100, ± 500 counts. Next, enable the pulse signal into all input channels, and make another correlator mode conversion. Read out all channels. The value should be around 2100, ± 500 counts. Note that the limits stated here would allow the first reading to 1600 (1100 + 500) and the second reading to be 1600 (2100 − 500) and still pass. That is ***not*** correct. In order to pass there must be a difference between the first and second measurement of 1000 ± 500 counts. Otherwise the die fails

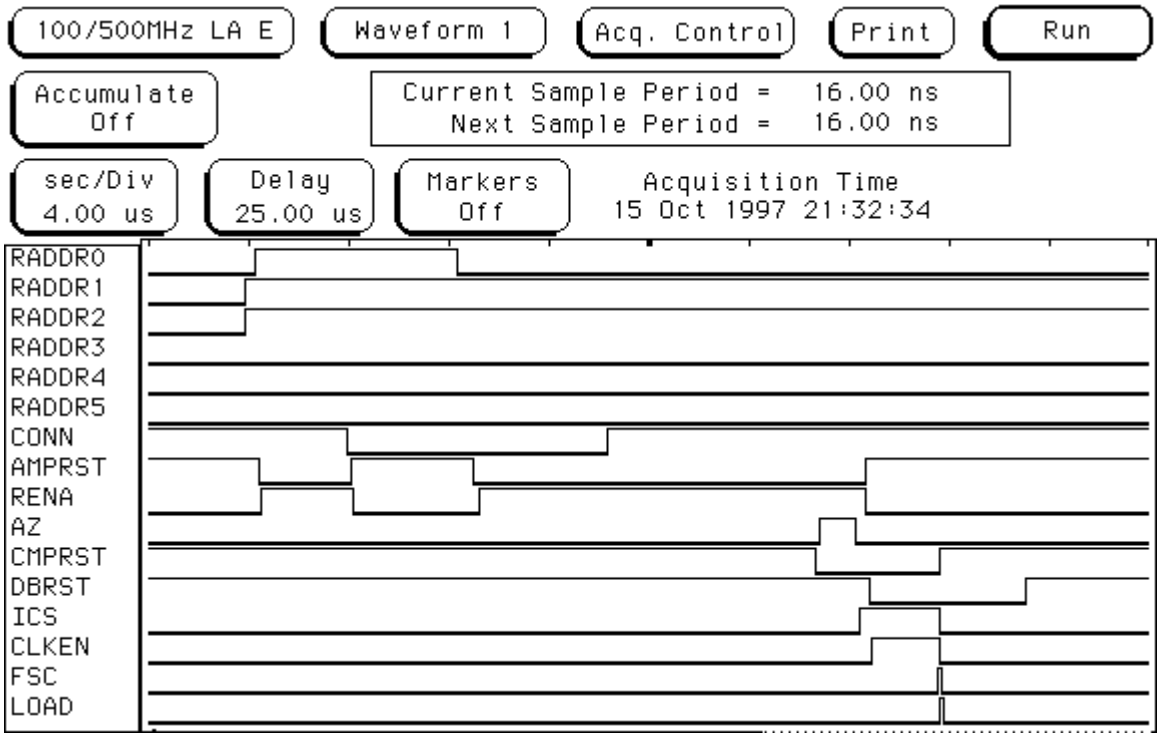
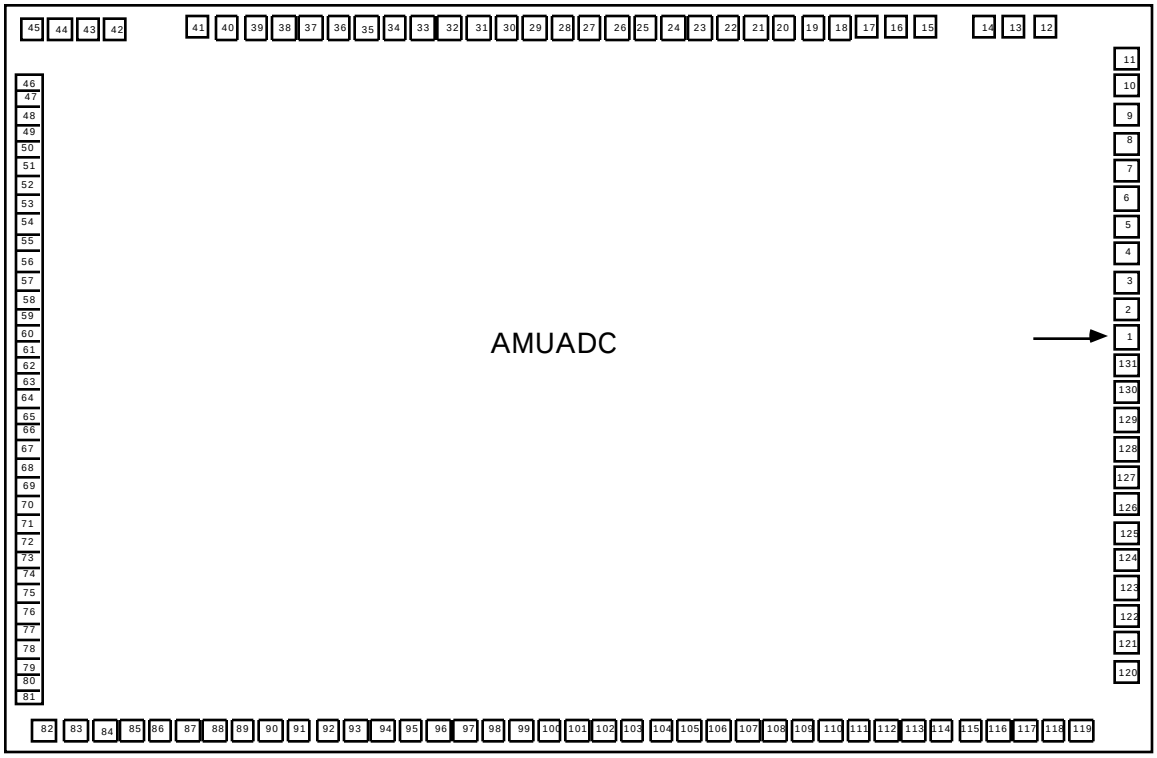


Figure 5. Operation using Correlator mode

SECTION 2. AMUADC PADFRAME.



Section 3. AMUADC Coordinate Table

Measurement of on Mon Kuly 7 15:40 1997
reference pads: 0 0
Rotation compensated for was 0.000000 radians
Outside dimensions x =6.748mm y = 4.532mm, z =0.000mmm
Pattern dimensions = x=6.68315mm, y=4.46775mm
Lower left pattern corner is x=.06465mm, y=.06425mm
from lower left chip silicon corner

Pad	Absolute	Relative to Pin 1
1	6.63904mm	2.43635mm
2	6.63904mm	2.60675mm
3	6.63904mm	2.77715mm
4	6.63904mm	2.94755mm
5	6.63904mm	3.11795mm
6	6.63904mm	3.28835mm
7	6.63904mm	3.45875mm
8	6.63904mm	3.62915mm
9	6.63904mm	3.79955mm
10	6.63904mm	3.96995mm
11	6.63904mm	4.14035mm
12	6.5262mm	4.42355mm
13	6.35584mm	4.42355mm
14	6.18544mm	4.42355mm
15	5.67424mm	4.42355mm
16	5.50384mm	4.42355mm
17	5.33344mm	4.42355mm
18	5.16304mm	4.42355mm
19	4.99264mm	4.42355mm
20	4.82224mm	4.42355mm
21	4.65184mm	4.42355mm
22	4.48144mm	4.42355mm
23	4.31104mm	4.42355mm
24	4.13884mm	4.42355mm
25	3.96844mm	4.42355mm
26	3.79804mm	4.42355mm
27	3.62764mm	4.42355mm
28	3.45724mm	4.42355mm
29	3.28684mm	4.42355mm

Pad	Absolute	Relative to Pin 1
30	3.11644mm	4.42355mm
31	2.94604mm	4.42355mm
32	2.77564mm	4.42355mm
33	2.60524mm	4.42355mm
34	2.43484mm	4.42355mm
35	2.26444mm	4.42355mm
36	2.09404mm	4.42355mm
37	1.92364mm	4.42355mm
38	1.75324mm	4.42355mm
39	1.58284mm	4.42355mm
40	1.41244mm	4.42355mm
41	1.24204mm	4.42355mm
42	.73264mm	4.42355mm
43	.56244mm	4.42355mm
44	.39184mm	4.42355mm
45	.22145mm	4.42405mm
46	.11675mm	4.16915mm
47	.11675mm	4.05755mm
48	.10835mm	3.94685mm
49	.10835mm	3.8382mm
50	.10835mm	3.7297mm
51	.10835mm	3.6211mm
52	.10835mm	3.51245mm
53	.10835mm	3.4038mm
54	.10835mm	3.2953mm
55	.10835mm	3.1867mm
56	.10835mm	3.07895mm
57	.10835mm	2.9694mm
58	.10835mm	2.8609mm
59	.10835mm	2.7523mm
60	.10835mm	2.64365mm
61	.10835mm	2.535mm
62	.10835mm	2.4265mm
63	.10835mm	2.3179mm
64	.10835mm	2.20925mm
65	.10835mm	2.1006mm
66	.10835mm	1.19921mm
67	.10835mm	1.8835mm
68	.10835mm	1.77485mm
69	.10835mm	1.6662mm
70	.10835mm	1.5577mm

Pad	Absolute	Relative to Pin 1
71	.10835mm	1.4491mm
72	.10835mm	1.34045mm
73	.10835mm	1.2318mm
74	.10835mm	1.1233mm
75	.10835mm	1.0147mm
76	.10835mm	.90605mm
77	.10835mm	.7974mm
78	.10835mm	.6889mm
79	.10835mm	.58025mm
80	.11675mm	.47075mm
81	.11675mm	.3591mm
82	.22145mm	.10835mm
83	.39184mm	.10835mm
84	.56224mm	.10835mm
85	.73264mm	.10835mm
86	.90304mm	.10835mm
87	1.07344mm	.10835mm
88	1.24384mm	.10835mm
89	1.41424mm	.10835mm
90	1.58464mm	.10835mm
91	1.75504mm	.10835mm
92	1.92544mm	.10835mm
93	2.09584mm	.10835mm
94	2.26624mm	.10835mm
95	2.43644mm	.10835mm
96	2.60704mm	.10835mm
97	2.77744mm	.10835mm
98	2.94784mm	.10835mm
99	3.11824mm	.10835mm
100	3.28864mm	.10835mm
101	3.45904mm	.10835mm
102	3.62944mm	.10835mm
103	3.79984mm	.10835mm
104	3.97024mm	.10835mm
105	4.14064mm	.10835mm
106	4.31104mm	.10835mm
107	4.48144mm	.10835mm
108	4.65184mm	.10835mm
109	4.82224mm	.10835mm
110	4.99264mm	.10835mm
111	5.16304mm	.10835mm

Pad	Absolute	Relative to Pin 1
112	5.33344mm	.10835mm
113	5.50384mm	.10835mm
114	5.67424mm	.10835mm
115	5.84464mm	.10835mm
116	6.01504mm	.10835mm
117	6.18544mm	.10835mm
118	6.35584mm	.10835mm
119	6.52625mm	.10835mm
120	6.63904mm	.39155mm
121	6.63904mm	.56195mm
122	6.63904mm	.73235mm
123	6.63904mm	.90275mm
124	6.63904mm	1.07315mm
125	6.63904mm	1.24355mm
126	6.63904mm	1.41395mm
127	6.63904mm	1.58435mm
128	6.63904mm	1.75475mm
129	6.63904mm	1.92515mm
130	6.63904mm	2.09555mm
131	6.63904mm	2.26595mm

Section 4.

TGV32 TESTING SPECIFICATION

Tony Moore
Oak Ridge National Lab

OVERVIEW

This document with its attachments comprises the specification of interfacing and testing requirements for the TGV32 preamplifier chip. This chip is a 32 channel CMOS charge sensitive preamplifier fabricated in a 1.2μ process. The approximate gain is 20 mV/femtocoulomb. Because of this sensitivity, it will be necessary to take particular care with the layout, construction , and cleaning of the probe/tester interface card. Input drive for testing is accomplished through a circuit called a charge terminator by the nuclear instrumentation engineering community. The charge terminator is simply a transmission line terminated in its characteristic impedance followed by a small (0.3pf in this case) high quality capacitor in series with the signal path. The input to the chip is held at ground potential by the chip's internal feedback so the entire voltage driving the transmission line appears across the series capacitor thus defining the amount of charge injected into the amplifier's input. This input coupling circuit will have to be incorporated into the probe card and physically positioned as closely as possible to the probe feed points. A microstrip configuration should be sufficient for the transmission line on the probe card. Shielded input probes are necessary to prevent signal contamination from 60Hz and other stray fields, but stray capacitance along the path from the 0.3 pf series capacitor to the chip input pad cannot exceed 10pf. This special configuration applies only to the 32 analog input pads, The probe card is conventional for the other 78 pads. The probe card must be cleaned thoroughly after soldering in order to eliminate DC leakage paths as the output error from stray leakage is 5μV per electron. All digital lines must be held static while analog measurements take place. Only the integrator reset lines are moved during analog
section testing. Tests are progressively complex, if a failure is detected subsequent tests on the chip will not be performed and the chip will be deemed defective.

CHIP POWER SUPPLIES

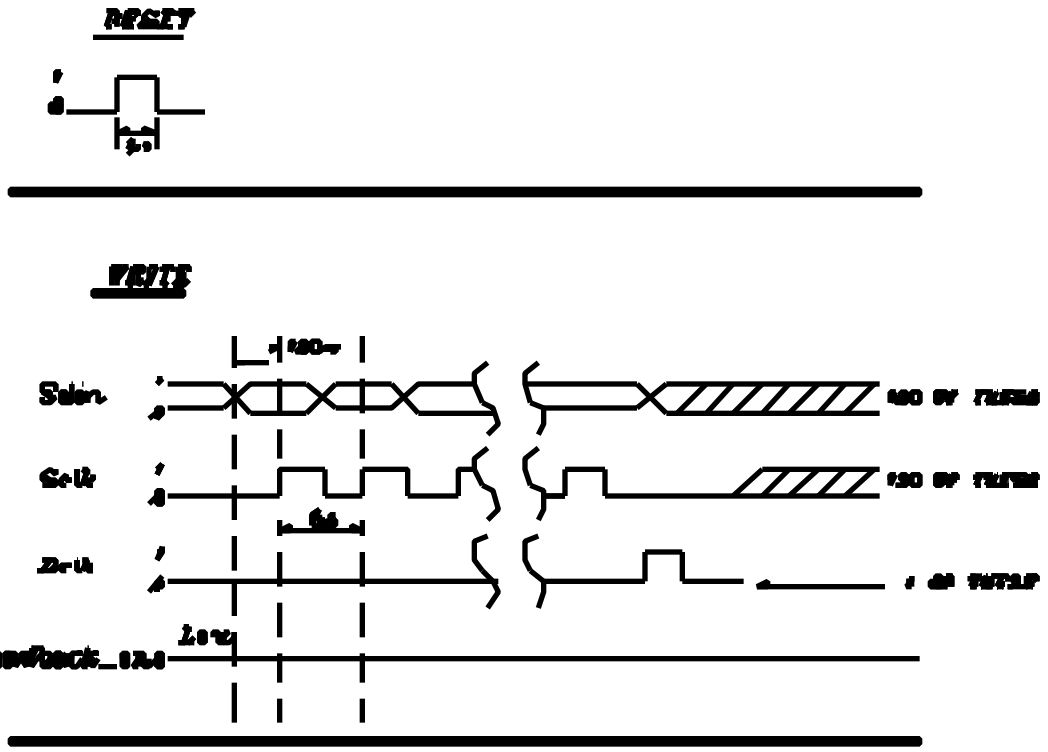
TGV32 requires three independent power supplies, all 5.0 volts DC. Pads 108, 110, 33, and 34 are Vdd_pre which is the preamplifier power supply. Pads 99, 89, 44, 53, 86, and 89 are Vdd_post which is the analog power for the remainder of the chip and requires 10μF of bypassing as near as possible to the chip . This chip's design affords essentially no power supply rejection so clean power is important for successful testing. Pads 96, 91, and 49 are Vdd_dig and is typical of any digital supply for CMOS circuits. The above power specification is used for all tests.

CONTROL COMMUNICATIONS

The TGV32 chip is configured by a 190 bit serial data stream which is written to or read from the chip by manipulation of five digital lines consisting of serial input and output lines, a shift clock line, a data latch line , and a read enable line. Bit one is the first bit in the serial string and bit 190 is the last whether reading or writing. Data is shifted in and latched on the rising edge of the shift clock and data clock lines respectively. Data setup time is 100 nsec, hold time is 20 nsec. Logic levels are standard 5 volt CMOS.

Bit #	Function
1-32	Channel 1-32 output current sum disable
33-96	Channel 32-1 discriminator tweak (2 bits per channel)
97-128	Channel 1-32 preamp disable
129-160	Channel 32-1 calibration enable
161-166	Discriminator threshold, MSB first, LSB last.
167-172	Vmid, MSB first, LSB last.
173-178	Vgate MSB first, LSB last.
179-184	Feedback resistor set voltage, MSB first, LSB last.
185-190	Calibration Voltage MSB first, LSB last.

COMMUNICATIONS PROTOCOL and TIMING



The shift clock frequency will be 1MHz nominally, pulses will be positive going with a duration between 90 to 110 nsec.

The communications test will consist of resetting the chip by sending a 1μS pulse to pad 48, then reading the chip configuration and verifying the following pattern (expressed in hexadecimal).
20FC,083F,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

NOTE the two MSB's are not actually sent or received since there are only 190 rather than 192 bits in the data stream. Only 190 cycles of the shift clock may be used or the data will be skewed and hence incorrect.

Write, latch, readback and verify the following pattern
2AAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA,AAAA

Next write, latch, readback and verify the following pattern
1555,5555,5555,5555,5555,5555,5555,5555,5555,5555,5555,5555

Reset chip (chip is reset by sending a 1μS pulse to, "reset" ,pad 48. This completes the communications test.

QUIESCENT CURRENT Note: tester maximum accuracy ± .005V

Write the following sequence to the chip, LSB first
20FC,083F,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

Measure the following currents ± 15%, (average of 5 readings) with 5.0V applied

PAD	CURRENT
108+110+33+34	.1345ma, no single pad to vary from .033 ma by more than 25%
99+89+44+53+86+89	7.8ma, no single pad to vary from 1.3ma by more than 25%
96+91+49	.0135ma, no single pad to vary from .0045ma by more than 25%

DAC and BIAS VOLTAGES

Write the following sequence to the chip LSB first (DACs = 3)
0618,6183,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

Measure the voltage on the following pads Note: tester maximum accuracy ± .005V

PAD	VOLTAGE
100	1.6 ± .2 V
101	1.93 ± .05V
104	.007 + .040, -.003 V
105	.006 ± .0015 V
106	4.24 ± .1 V

Write the following sequence to the chip LSB first (DACs = 20)
1451,4514,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

PAD	VOLTAGE
100	2.6 ± .2 V
101	1.75 ± .05V
104	1.5 ± .5 V
105	.95 ± .1 V
106	4.6 ± .1 V

Write the following sequence to the chip LSB first (DACs = 40)
28A2,8A28,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

PAD	VOLTAGE
100	3.5 ± .2 V
101	1.53± .05V
104	3.5 ± .5 V
105	2.28 ± .1 V
106	4.95 ± .03 V

Write the following sequence to the chip LSB first (DACs = 50)
32CB,2CB2,0000,0000,0000,0000.0000,0000,0000,0000,0000,0000

PAD	VOLTAGE
100	4.0 ± .2 V
101	1.38± .05V
104	4.5 ± .5 V
105	2.95 ± .1 V
106	4.95 ± .03 V

OUTPUT OFFSET

Write the following sequence to the chip LSB first (DACs = 50)
32CB,2CB2,0000,0000,FFFF,FFFF,0000,0000,0000,0000,0000,0000

The voltage at vout1-vout32 (pads 85-54) shall be 1.25±.1 V

CHANNEL GAIN and RISE TIME

Write the following sequence to the chip LSB first
41F,8083,0000,0000,0000,0000,0000,0000,0000,0000,0000,0000

Send simultaneous 100 µs long pulses to pre_reset (pad 42) and s2_reset (pad 43), wait 2µs and send a -100mV pulse with a duration of 10 µs and a fall time <10ns simultaneously to odd numbered pads qin1 - qin32 (pads 1-32). The gain measured to odd numbered pads vout1-vout32 (pads 85-54) shall be -9 ± 1. The 10-90% rise time of the output step shall be < 100ns. The gain to the even numbered pads shall be less then 2. Repeat the test driving even numbered pads insuring the same gains to corresponding and adjacent outputs.

The approach envisioned is to use the tester's logic analysis function to determine that the output has moved from its pre-pulse level to a level 900mV ± 100mV greater. This might require two test cycles verifying that a pulse greater than 800mV occurred but that a pulse greater than 1V did not occur, and that the output pulse reached 800mv less than 100ns after initiation of the drive pulse. It is hoped that "clever" use of digital test functions such as this would allow simultaneous testing of the 32 channels and significantly reduce test time and cost.

DISCRIMINATOR and CALIBRATION

Write the following sequence to the chip LSB first
14FE,F823,FFFF,FFFF,0000,0000,0000,0000,0000,0000,0000,0000

Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43), at the end of the reset pulses send a 30 μs long pulse to calibrate_bar (pad 41) on the falling edge of this pulse a current pulse of more than 300 μA should occur within 100 nsec at idiscout (pad 46).

Write the following sequence to the chip LSB first
14FE,F823,FFFF,FFFF,0000,0000,0000,0000,0000,0000,FFFF,FFFF

Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43), at the end of the reset pulses send a 30 μs long pulse to calibrate_bar (pad 41) on the falling edge of this pulse no current may occur within 100 nsec at idiscout (pad 46).

Write the following sequence to the chip LSB first
14FE,F823,AAAA,AAAA,0000,0000,0000,0000,0000,0000,0000,0000

Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43), at the end of the reset pulses send a 30 μs long pulse to calibrate_bar (pad 41) on the falling edge of this pulse a current pulse of more than 150 μA should occur within 100 nsec at idiscout (pad 46).

Write the following sequence to the chip LSB first
14FE,F823,5555,5555,0000,0000,0000,0000,0000,0000,0000,0000

Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43), at the end of the reset pulses send a 30 μs long pulse to calibrate_bar (pad 41) on the falling edge of this pulse a current pulse of more than 150 μA should occur within 100 nsec at idiscout (pad 46).

Write the following sequence to the chip LSB first
14FE,F83F,FFFF,FFFF,0000,0000,0000,0000,0000,0000,0000,0000

Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43), at the end of the reset pulses send a 30 μs long pulse to calibrate_bar (pad 41) on the falling edge of this pulse a current pulse of less than 25 μA is permissible within 100 nsec at idiscout (pad 46). No pulse at all is expected.

NOISE

Noise from each channel will be evaluated by determining the mean-square value of the band limited noise component of the output signal over a data set of 190 points derived from 20 analog samples taken at 400ηS intervals. Each data point will be squared and added to an accumulated sum of the previous squared points. When all have been squared and added, the sum will be divided by the number of points (190). Also the data points will be averaged in the common fashion. The resultant average will be squared and subtracted from the quotient of the squared data points previously computed. The remainder after subtraction is the mean-square noise for that channel which must be lower than the specified threshold. The 190 points will be derived from the 20 samples by taking the unique difference between each sample and every other sample by the following process:

$D_1=(S_1-S_2)$, $D_2=(S_1-S_3)$, $D_{3=}(S_1-S_4)$ … $D_{19}=(S_1-S_{20})$

$D_{20}=(S_2-S_3)$, $D_{21}=(S_2-S_4)$, … $D_{37}=(S_2-S_{20})$

.
.

.

$D_{188}=(S_{18}-S_{19})$, $D_{189}=(S_{18}-S_{20})$

$D_{190}=(S_{19}-S_{20})$.

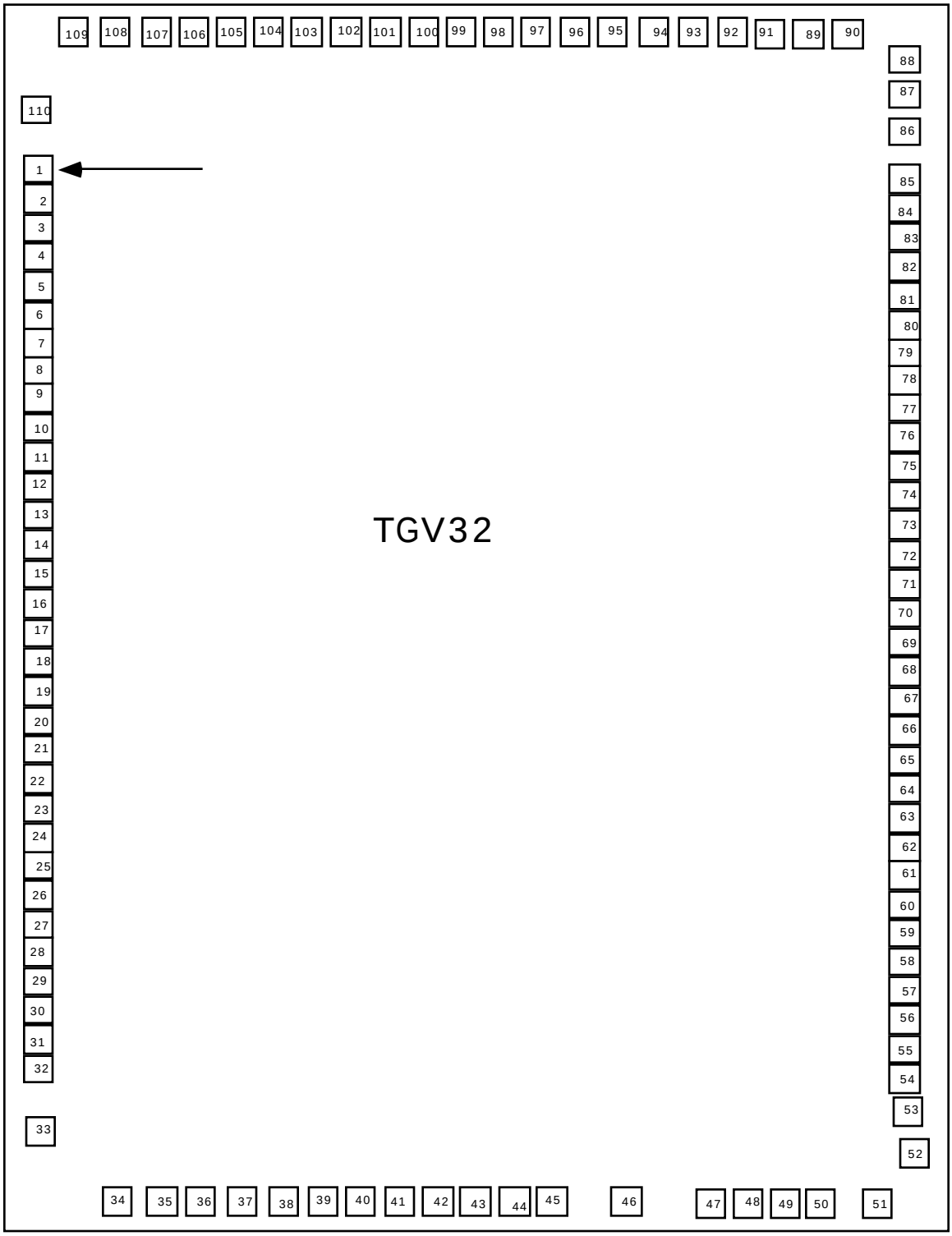
The acceptable value will be approximately $25\mu V^2$ or less. This process will be repeated for all 32 channels.

Procedure:

Send a reset pulse to reset (pad 48). Send simultaneous 100 μs long pulses to pre_reset (pad 42) and s2_reset (pad 43). Wait 5μS then using the Video Digitizer Card of the DUO tester, take 20 successive 12 bit samples at 400ηS intervals of the output from channels 1-4 (pads 85-82). This procedure assumes that all four channels are sampled simultaneously or nearly so and that all 80 samples can be acquired and converted in 40μS. Compute the mean-square noise for channels 1 through 4 and compare to the acceptable value (to be determined).

Omit the reset pulse to pad 48 and repeat the above procedure for channels 5-32 (pads 81-54). Should the tester have capability to do more than 4 channels at a time, up to all 32 channels may be done simultaneously.

Section 5. TGV32 Padframe



Section 6. TGV32 Pad Coordinate Table

Measurement of TGV32 on Mon Oct 20 9:11 1997
Reference pads: 52 110
Rotation compensated for was 0.000000 radians
Outside dimensions x = 4.200mm, y= 4.646mm, z=0.540mm
Pattern dimensions x=4.051mm, y=4.517mm
Lower left corner is x=0.07257mm, y=0.06272mm
from lower left chip silicon corner

Pad	Absolute	Relative to Pin 1
54	4.0521mm	0.6847mm
55	4.0521mm	0.7849mm
56	4.0521mm	0.8851mm
57	4.0521mm	0.9853mm
58	4.0521mm	1.0855mm
59	4.0521mm	1.1857mm
60	4.0521mm	1.2859mm
61	4.0521mm	1.3861mm
62	4.0521mm	1.4863mm
63	4.0521mm	1.5865mm
64	4.0521mm	1.6867mm
65	4.0521mm	1.7869mm
66	4.0521mm	1.8871mm
67	4.0521mm	1.9873mm
78	4.0521mm	2.0875mm
69	4.0521mm	2.1877mm
70	4.0521mm	2.2879mm
71	4.0521mm	2.3881mm
72	4.0521mm	2.4883mm
73	4.0521mm	2.5885mm
74	4.0521mm	2.6887mm
75	4.0521mm	2.7889mm
76	4.0521mm	2.8891mm
77	4.0521mm	2.9893mm
78	4.0521mm	3.0895mm
79	4.0521mm	3.1897mm
80	4.0521mm	3.2899mm
81	4.0521mm	3.3901mm
82	4.0521mm	3.4903mm
83	4.0521mm	3.5905mm
84	4.0521mm	3.6906mm

Pad	Absolute	Relative to Pin 1
85	4.0521mm	3.7909mm
86	4.0815mm	3.9262mm
87	4.0815mm	4.0972mm
88	4.0815mm	4.2669mm
89	3.7803mm	4.5376mm
90	3.6093mm	4.5376mm
91	3.4395mm	4.5376mm
92	3.2691mm	4.5376mm
93	3.0987mm	4.5376mm
94	2.9283mm	4.5376mm
95	2.7579mm	4.5376mm
96	2.5875mm	4.5376mm
97	2.4171mm	4.5376mm
98	2.2473mm	4.5376mm
99	2.0763mm	4.5376mm
100	1.9059mm	4.5376mm
101	1.7355mm	4.5376mm
102	1.5651mm	4.5376mm
103	1.3947mm	4.5376mm
104	1.2243mm	4.5376mm
105	1.0539mm	4.5376mm
106	.8835mm	4.5376mm
107	.7131mm	4.5376mm
108	.5427mm	4.5376mm
109	.3723mm	4.5376mm
110	.1479mm	4.1818mm
1	.1479mm	3.7909mm
2	.1479mm	3.6907mm
3	.1479mm	3.5905mm
4	.1479mm	3.4903mm
5	.1479mm	3.3901mm
6	.1479mm	3.2899mm
7	.1479mm	3.1897mm
8	.1479mm	3.0895mm
9	.1479mm	2.9893mm
10	.1479mm	2.8891mm
11	.1479mm	2.7889mm
12	.1479mm	2.6887mm
13	.1479mm	2.5885mm
14	.1479mm	2.4883mm
15	.1479mm	2.3881mm

16	.1479mm	2.2879mm
17	.1479mm	2.1877mm
Pad	**Absolute**	**Relative to Pin 1**
18	.1479mm	2.0875mm
19	.1479mm	1.9873mm
20	.1479mm	1.8871mm
21	.1479mm	1.7869mm
22	.1479mm	1.6867mm
23	.1479mm	1.5865mm
24	.1479mm	1.4863mm
25	.1479mm	1.3861mm
26	.1479mm	1.2859mm
27	.1479mm	1.1857mm
28	.1479mm	1.0855mm
29	.1479mm	.9853mm
30	.1479mm	.8851mm
31	.1479mm	.7849mm
32	.1479mm	.6897mm
33	.1479mm	.4642mm
34	.3723mm	0.1084mm
35	.5427mm	0.1084mm
36	.7131mm	0.1084mm
37	.8835mm	0.1084mm
38	1.0539mm	0.1084mm
39	1.2243mm	0.1084mm
40	1.3947mm	0.1084mm
41	1.5651mm	0.1084mm
42	1.7355mm	0.1084mm
43	1.9059mm	0.1084mm
44	2.0763mm	0.1084mm
45	2.2473mm	0.1084mm
46	2.5875mm	0.1084mm
47	2.9283mm	0.1084mm
48	3.0987mm	0.1084mm
49	3.2691mm	0.1084mm
50	3.4395mm	0.1084mm
51	3.7803mm	0.1084mm
52	4.0815mm	.3784mm
53	4.0815mm	.5794mm

Section 7. TGV32 Pad decsription/identification table

Tgv32bh Pad Definitions
Rev D. (8/29/97)
(Note: These apply to the t32bh chip revision ONLY)

SIGNALS

qin1-32 - Charge inputs from detectors.

vout1-32 - Voltage outputs from preamplifier channels.

calibrate_bar - Normally low. After calibration pattern is loaded, pin is changed to high for pre-charge and then low for actual calibration voltage output.

pre_bias - Output of preamplifier bias point. Needs to have filter capacitor (1uF).

pre_reset - Preamplifier reset. Normally low. Reset occurs when high.

s2_reset - Stage 2 reset. Normally low. Reset occurs when high.

s2_bias - Output of stage 2 bias point. Needs to have filter capacitor (1uF).

discbias_1 - Discriminator bias output.

discbias_2 - Discriminator bias output.

ibias - Current output bias point.

idiscout - Multiplicity current output. Approx. 50μA/channel.

readback_en - Normally low. After data is loaded, this line is forced high for one full **sclk** pulse. The line is then forced low. The readback is then accomplished by continuously pulsing **sclk**.

reset - Normally low. Master shift-logic reset when high.

sdout - Output of serial string stored data.

vcal - Monitor point of calibration voltage.

vgate - Monitor point for discriminator gate voltage.

vfb_res - Monitor point for preamplifier feedback resistor control voltage.

sdin - Input for serial string data.

dac_bias - Output of dac bias point.

dac_vmid - 2.5 volt input for dac bias.

disc_vmid - Monitor point for discriminator midpoint voltage.

ithresh - Monitor point for discriminator threshold bias.

dclk - Normally low. Positive edge clocks serial data into data registers.

sclk - Normally low. Positive edge clocks serial data into shift registers.

dac_amp_bias1 Bias point output for vcal and vfb_res dacs.

dac_amp_bias2 Bias point output for vgate and disc_vmid, and ithresh dacs.

POWER

vdd_dig - Digital +5V.

vss_dig - Digital GND.

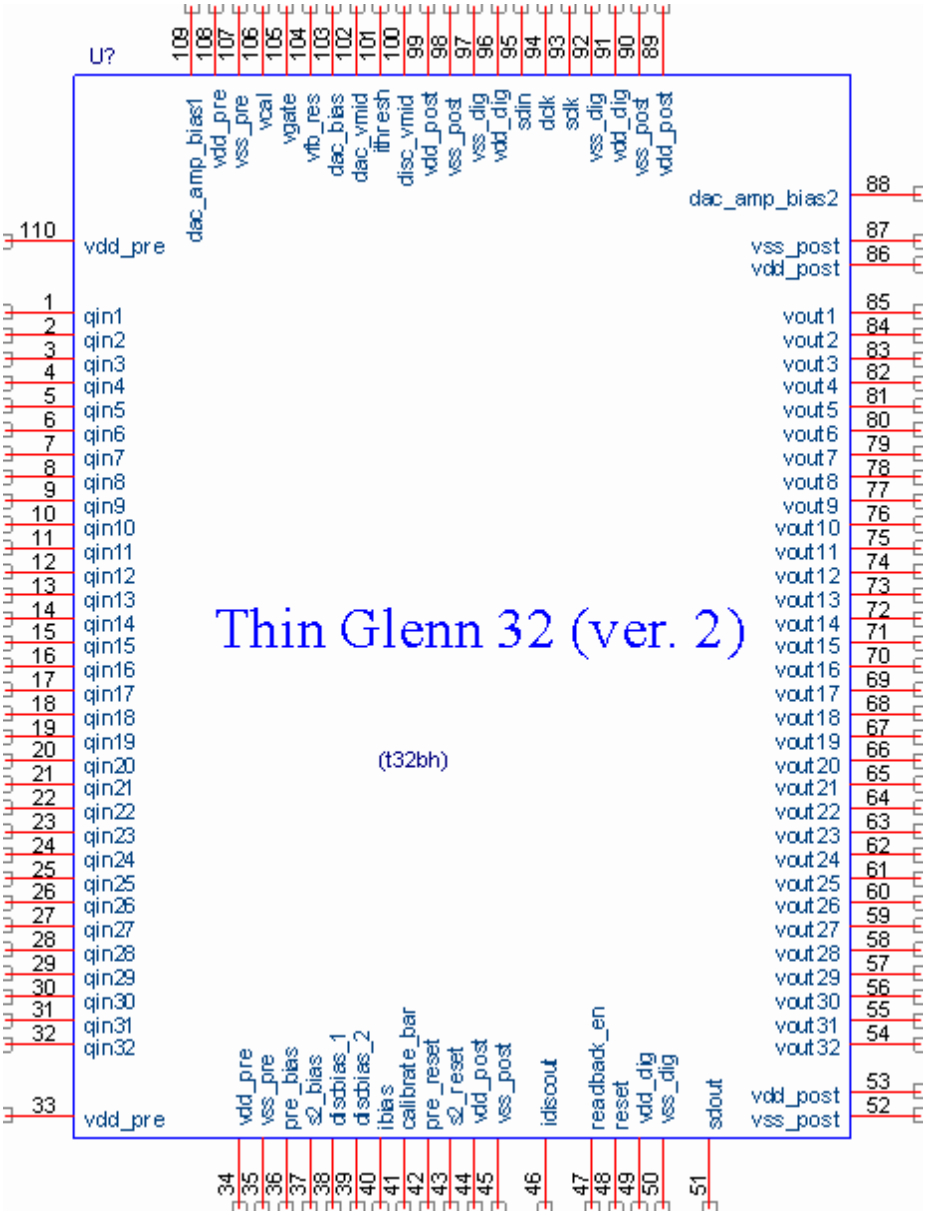
vdd_pre - Preamplifier and detector return +5V.

vss_pre - Preamplifier GND.

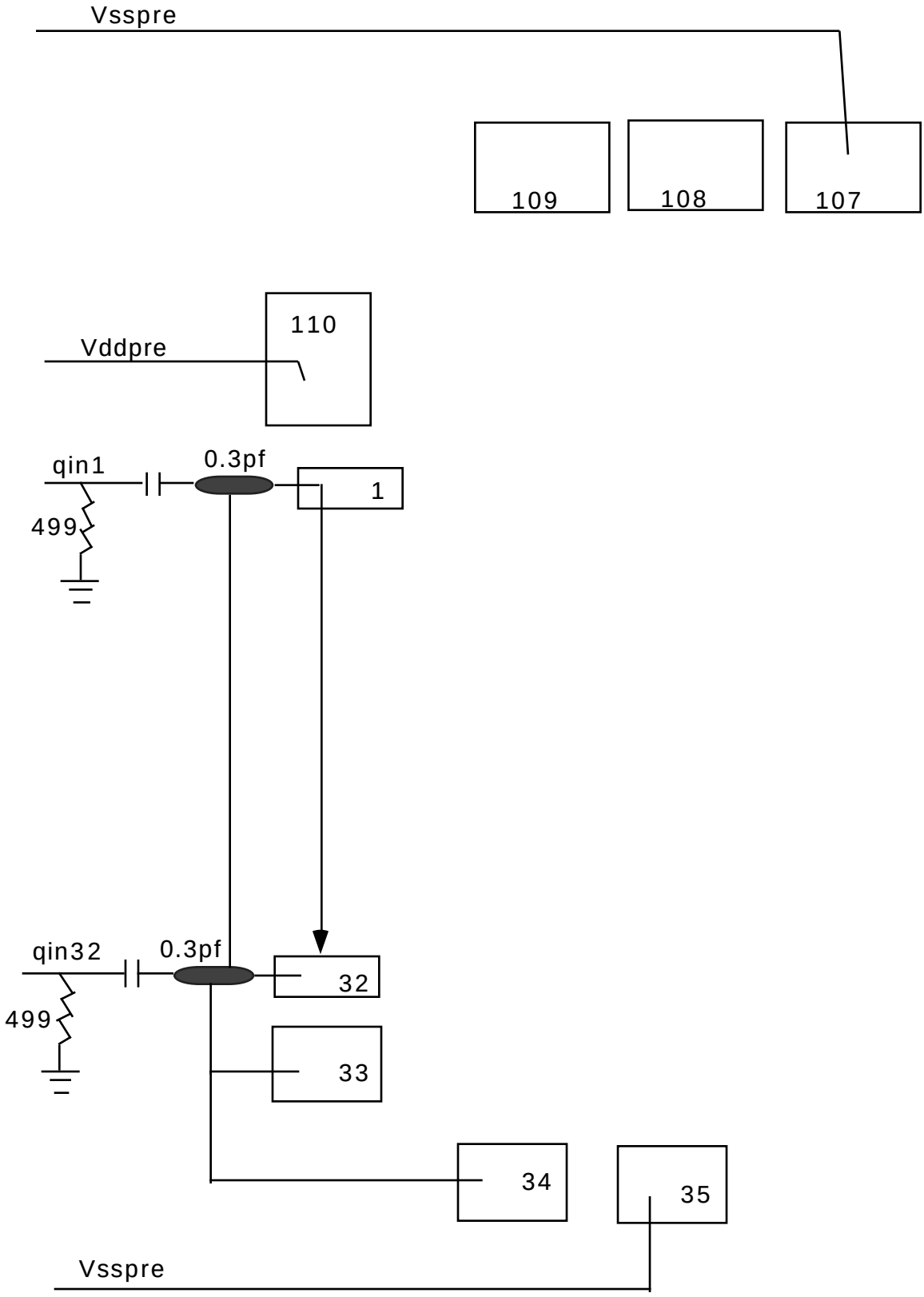
vdd_post - 2^{nd} stage, discriminator, and pad frame +5V.

vss_post - 2^{nd} stage, discriminator, and pad frame GND.

TGV32 Pad Identification and Orientation Diagram



Section 8. TGV32 probe card configuration sketch



Section 9. Cover Letter to ISE

Dear Adi;

I guess you were beginning to wonder if we were really serious about the testing job we have been discussing. Well we actually are, and finally have enough information collected to request a quotation. We are currently planning to forego burn in of the chips and execute final testing at wafer probe then saw the wafers into individual die, visually inspect them for damage during sawing and ship the MCM fabricator. Since under this plan there are no tests after sawing, the visual inspection is critical and must be done with patience and great care.

We have two different chips to test. The first chip tested will be the AMU/ADC. The signal levels and probing for this chip are conventional. The second chip will be the TGV32 which is a preamplifier requiring some careful shielding of the 32 analog inputs as well as some general shielding above the die. We request a separate itemized quotation for each chip to include all probing fixtures associated with interfacing the chips at wafer probe to the tester; programming of the tester in accordance with the attached test specifications, execution of the tests; sawing the wafers; careful visual and dimensional inspection of each die after sawing, and packaging the good die for shipment to the MCM fabricator. The Quotation should be for testing 3,200 AMU/ADC die with the option of testing an additional 18,400 die for communication and power consumption only during the same test run. The TGV32 quotation should be for complete testing of 3,200 die. In the unlikely event that 1600 good die are not obtained after testing 3200 die, testing will continue until 1600 good die are obtained, and the same applies to AMUADC. We anticipate providing an engineer at your site to help with startup of the testing and to establish final acceptance tolerances on your test fixture. We should also be consulted on the TGV32 probe card design before committing to fabrication. We are willing if need be to send an engineer to your facility to work with your staff on the probe card design / shielding scheme. We are open to any criticism or suggestions you may wish to offer that your experience indicates would improve our end result or that would offer savings of time or money.

The die will be on 6" diameter wafers from HP's 1.2µ analog CMOS process. There will be 60 wafers of AMU/ADC and 20 wafers of TGV32. AMUADC will have 360 die per wafer and TGV32 will be close to that. Tested wafers will be sawed to a finished size of 4532µ X 6748µ for AMU/ADC and 4200µ X 4646µ for TGV32.During visual inspection it will be necessary to verify the die size. AMU/ADC die must be no larger than 4557µ X 6770µ nor smaller than 4510µ X 6725µ. TGV32 die must be no larger than 4225µ X 4670µ nor smaller than 4175µ X 4625µ.

The wafers remaining after testing the required number of die will be returned untested. As soon as any die fails a test it will be identified as defective and any remaining tests for that die will be skipped. Bad die will be returned, but do not require any care in, handling and packaging or separation from each other. We are allowing for a 50% yield however the observed yield on our prototype runs has been above 90%.

The test specifications are organized by the functionality to be tested and by increasing complexity. The test specifications are in no way intended to restrict the parallel testing capability of the tester, The tester should be programmed in such a way as to maximize throughput executing as many tests simultaneously as is practicable.