Design and Performance of Beam Test Electronics for the PHENIX Multiplicity Vertex Detector[1]

C. L. Britton, Jr., W. L. Bryan, M. S. Emery, M. N. Ericson, M. S. Musrock, M. L. Simpson, M. C. Smith, J. W. Walker, A. L. Wintenberg, G. R. Young
Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831-6006

M. D. Allen, L. G. Clonts, R. L. Jones, E. J. Kennedy, R. S. Smith
The University of Tennessee, Knoxville, Tennessee 37996-2100

J. Boissevain, B. V. Jacak, D. Jaffe, J. S. Kapustinsky, J. Simon-Gillo, J. P. Sullivan, H. Van Hecke, N. Xu
Los Alamos National Laboratory, Los Alamos, New Mexico 87545

Abstract

The system architecture and test results of the custom circuits and beam test system for the Multiplicity-Vertex Detector (MVD) for the PHENIX detector collaboration at the Relativistic Heavy Ion Collider (RHIC) are presented in this paper. The final detector per-channel signal processing chain will consist of a preamplifier-gain stage, a current-mode summed multiplicity discriminator, a 64-deep analog memory (simultaneous read-write), a post-memory analog correlator, and a 10-bit 5 μs ADC. The Heap Manager provides all timing control, data buffering, and data formatting for a single 256-channel multi-chip module (MCM). Each chip set is partitioned into 32-channel sets. Beam test (16-cell deep memory) performance for the various blocks will be presented as well as the ionizing radiation damage performance of the 1.2 μm n-well CMOS process used for preamplifier fabrication.

I. Introduction

The requirements of low-power consumption, small physical area, a channel count of approximately 34,000, and flexible data handling make the MVD of the PHENIX detector at RHIC one of the most challenging of the PHENIX detector subsystems [1]. Additional requirements, which include a minimum 10:1 system signal-to-noise ratio for a single Minimum Ionizing Particle (MIP) signal (which results in noise less than 2500 electrons rms) and discrimination of a 0.25 MIP event for the per-channel multiplicity discriminator, offer a challenging set of problems.

The MVD is a 2-layer barrel detector comprised of 112 strip detectors and 2 disk-shaped end caps comprised of 24 wedge-shaped pad detectors. It is a clam-shell design, constructed in two halves to close about the beam pipe. The main physics goals of the detector are to provide a multiplicity measurement to the PHENIX Level-1 trigger, and to reconstruct the collision vertex to better than 2 mm.

There are a variety of silicon readout systems in the literature. The majority of systems read out events on the silicon strips with a preamplifier and discriminator [2, 3, 4, 5]. Some newer systems are planning to use analog readout [6, 7, 8, 9, 10, 11]. The MVD readout is a hybrid of both. It uses analog information for the primary vertex-finding information and a discriminator for the multiplicity information.

This paper presents measurements of the prototype circuits including the preamplifier-discriminator, analog memory unit (AMU), analog-digital converter (ADC) and Heap Manager for the MVD detector front-end electronics (FEE). The system was run in the BNL AGS facility as a fixed-target experiment. The electronics, however, were run as simultaneous read-write with a sampling rate of 400 ns.

II. Electronics Architecture

A block diagram of the electronics is shown in Figure 1. This includes the preamplifier, discriminator, current-sum output, analog memory-correlator and ADC. The system controller, or Heap Manger, is not shown but will also be discussed.

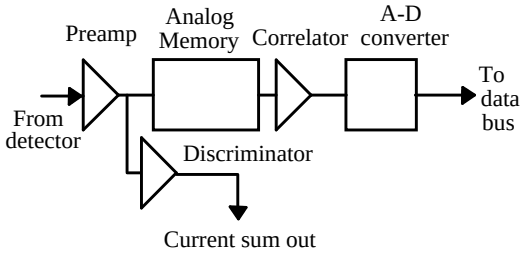

Figure 1: System block diagram.

The electronics will be mounted on a MCM. Each MCM will be connected to a 256-channel strip detector and will contain 8 preamplifier-discriminator chips and 8 analog memory-ADC chips. Each of these chips will contain 32 channels of its respective functions. In addition, the MCM

[1]Research sponsored by the U.S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corporation for the U.S. Department of Energy under Contract No. DE-AC05-96OR22464.

will contain the Heap Manager chips and associated control logic. In the prototyping/beam test round, we have fabricated an 8-channel die set. The beam test chip set consisted of an 8-channel preamplifier, and 8-channel AMU with a 16-cell depth, and an 8-channel ADC. Eight of each of the chips were used for a total of 64 channels. The beam test sampling rate was 2.5 MHz.

A. Preamplifier

The preamplifier, shown in Figure 2, utilizes a PMOS cascode amplification stage for low 1/f noise. The input device operates in weak inversion with a drain current of 100 µA. Versions of this design are presently being used by not only PHENIX, but also by the PHOBOS detector collaboration [12] (also at RHIC), and the Naval Research Laboratories (NRL) for Germanium spectroscopy [13]. The PHENIX version employs a wideband gain stage after the preamplifier. The resultant power dissipation of the PHENIX preamplifier is approximately 1.2 mW. The circuit is fabricated in 1.2 µm n-well CMOS and has an 85 µm/channel pitch.

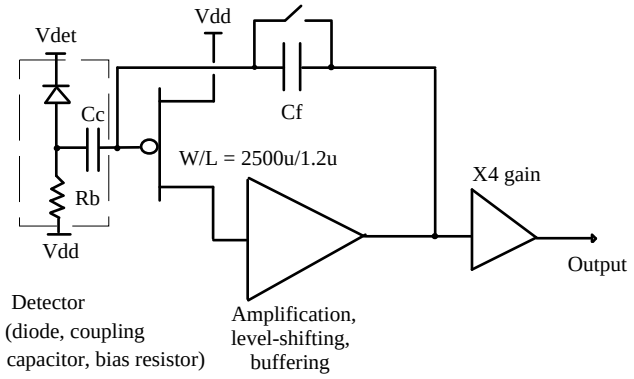

Figure 2: Preamplifier and detector block diagram.

The preamplifier has a dynamic range of 75 fC which corresponds to a full scale output voltage of 1.5V and a signal range of 19 MIPs. This range was chosen because the expected charge deposited in a single strip in one reset period (1 ms) for a Si-Cu beam is 7 MIPS. A factor of at least two above this maximum was chosen to ensure linear operation for even unforeseen operating conditions. The integral non-linearity over a 12.5 MIP input range (~1V) is +0.3% and -0.1%, most adequate for the application. The measured preamplifier risetime is 29 ns at 0 pF and 41 ns at 10 pF versus simulations of 26 ns and 44 ns respectively. The measured double-correlated rms noise (225 ns difference time) of the preamplifier is 590 e at 0 pF and 910 e at 10 pF (slope = 32 e/pF) versus simulations of 524 e and 1112 e respectively. We have experienced such discrepancies with our noise simulations before and are presently in the process of deriving new noise models.

The detector, shown in dotted line, has an ac-coupling capacitor equal to approximately 150 pF and a bias resistor equal to approximately 5 MΩ. This configuration, when combined with the preamplifier, exhibits a noise transfer function equal to

$$\overline{e^2_{output}} = \frac{1}{2\pi}\int_0^\infty E^2_{in}\left|\frac{C_c}{C_f}\cdot\frac{\left(1+sC_f R_b\right)}{\left(1+sC_c R_b\right)}\right|^2 d\omega . \quad (1)$$

E^2_{in} (ignoring flicker noise) is defined as [14]

$$E^2_{in} = \frac{8\cdot k\cdot T\cdot n}{3\cdot g_m}\Delta f, \quad (2)$$

where n is the subthreshold slope and g_m is the device transconductance. If we add a feedback resistor across the feedback capacitor, the transfer function becomes

$$\overline{e^2_{output}} = \frac{1}{2\pi}\int_0^\infty E^2_{in}\left|\frac{1+sC_c R_f + s^2 C_f R_f C_c R_b}{(1+sC_f R_f)(1+sC_c R_b)}\right|^2 d\omega . \quad (3)$$

At low frequencies, Eq. (3) clearly predicts less noise than (1) because $C_f << C_c$. While these equations give some insight into the effects of the components, they are difficult to use when including all effects such as the 1/f noise of the transistors, finite open-loop gain of the preamplifier, etc.

The correlated sampling present in the analog memory reduces the low frequency noise, but does nothing to effect the preamplifier directly. Unexpected noise spikes due to detector pickup or power line variations can have the effect of overloading the preamplifier and driving the output of the preamplifier into a nonlinear region. In order to understand the contribution of the feedback resistor to noise at the output of the preamplifier, the circuit was simulated in HSPICE and the signal/noise for a variable feedback resistor was plotted. The detector capacitance was 10 pF, C_c was equal to 200 pF, and R_b was as previously stated. The signal/noise ratio for the preamplifier both before (S/N direct) and after (S/N DCS) an ideal double-correlator are plotted as a function of the feedback resistor in Figure 3.

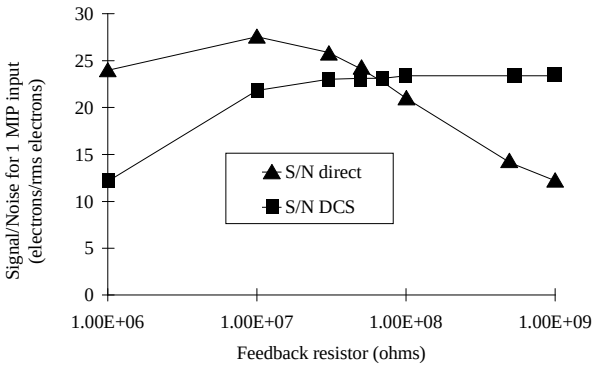

Figure 3: Signal/noise vs. Feedback resistor.

The results indicate that a feedback resistor between 10 MΩ and 100 MΩ results in approximately the same S/N ratio for both correlated sampling and direct output. This range is an acceptable compromise between having good double-correlated performance and limiting the effects of low-frequency noise pickup. For the beam test, the feedback switch, which is a pMOS FET, was biased on at all times and adjusted for minimum overall system noise. The final version of the preamplifier has a long channel (W=1.8 μm, L=200 μm) pMOS FET in the feedback which will allow an appropriate adjustment of the feedback time constant.

B. Discriminator

The multiplicity discriminator [15] block diagram is presented in Figure 4. Each time an input step greater than the threshold setting is detected, a fixed-value current source is switched to a summing node. The current-mode outputs of 256 discriminators are summed in this manner to produce a multiplicity output whose amplitude is proportional to the number of fired discriminators. The resultant current sum is buffered by a transimpedance amplifier and input to a flash ADC for the multiplicity count.

The design allows triggering at every beam crossing (108 ns) with no deadtime and has a total power consumption of approximately 500 μW/channel. The beam test version of the discriminator had a limited adjustment range of between 20 mV and 40 mV. A modification has been made to the design which now allows the range to be adjusted to 20 mV - 250 mV. The input channel-channel variation is now +/-5 mV by employing a serially programmed adjustment on each channel.

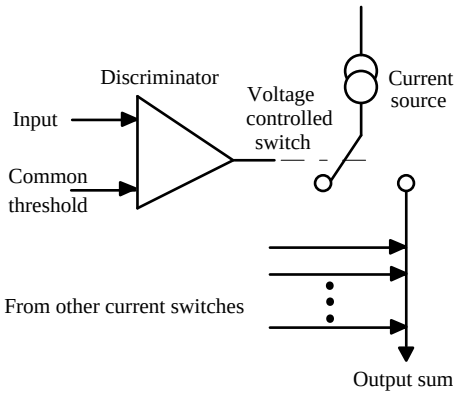

Figure 4: Block diagram of the discriminator.

C. Analog memory-correlator

The final analog memory unit (AMU) is a 64-cell deep, voltage-write-voltage-read, deadtime-less topology with a power dissipation of approximately 1 mW/channel. The beam test electronics utilized a 16-cell deep prototype version that had the same cell design and output amplifier as the larger unit. The memory is followed by an analog correlator that performs the double-correlated sampling. Both direct memory output and correlated output are available to the subsequent analog-digital converter (ADC). The memory reading and writing is addressed externally from the Heap Manager. The read and write logic decoders are completely independent to allow simultaneous read-write (deadtime-less) operation. A block diagram of the memory is presented in Figure 5. Due to time constraints in the software development, the correlator was not used in the beam test. The data was subtracted off line. The pedestal variations for the memory without the preamplifier were not measured, but the memory alone in a stop and read mode was measured to be between 0.7 mV-1 mV rms for a 10 MHz sampling rate. The integral nonlinearity was measured to be +0.05 % and -0.03 % between 0.25V and 4.75 V output range. The measured gain of the memory was found to be approximately 0.99 V/V.

The memory was originally fabricated with a 1.2 μm n-well process. Recently, tests were performed to measure the amount of dielectric absorption [16] present in the particular process. Dielectric absorption (DA) will cause a trigger latency-dependent degradation of the charge stored on the memory storage capacitor. Some testing by other collaborators [17] had indicated the process exhibited significant DA. Our testing revealed that there is indeed some DA at approximately the 10-11 bit level. This is a marginal effect for the MVD subsystem but it could be a serious problem for the calorimeters and other subsystems within the detector. Because we are planning to use this memory for all subsystems, the decision was made to fabricate in another 1.2 μm n-well process. This process was tested by both ORNL and Nevis Laboratory and found to have DA equal to or less than 1 part in 4000 (12 bits).

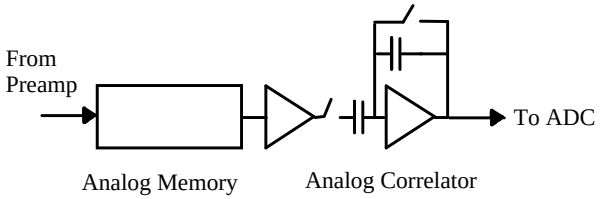

Figure 5: Memory block diagram.

D. Analog-digital converter

To allow easy maintainability and take advantage of the economics of scale, the readout architecture of the subsystems within the PHENIX detector have been designed to resemble one another. A universal AMU/ADC chip that will be used in several PHENIX subsystems is currently being designed. The architecture of the chip is 32 channels of 64-deep AMU and 32 channels of switchable 9-, 10-, 11-, 12-bit ADC. Due to dynamic range requirements, the MVD ADC will be set for 10-bit operation. The ADC has an adjustable dynamic range of up to 4.5 Volts. The prototype chip implements an eight channel version of the ADC [18, 19]. The circuit dissipates 1.19 mW/channel for the 8-channel prototype at 100 MHz clock frequency (5 μs conversion time for 10-bit conversions).

To measure Integral Nonlinearity (INL), precisely known voltages were applied to the input. The results of several ADC

conversions were then averaged. A least-squares curve fit was then performed for the input voltage versus averaged ADC value. Figure 6 shows the INL obtained by plotting the percentage difference of the ADC value from the best-fit line. The INL was less than 0.03% with an 80 MHz clock.

The Differential Nonlinearity (DNL) was measured by supplying a slowly varying triangle waveform to the ADC input with a peak to peak amplitude that just exceeded the conversion range of ADC and allowing conversions to be made at a regular period for a sufficiently long time to collect enough data to be statistically significant. The data consisted of a histogram of the number of times each ADC code was hit. DNL was found from the percent difference of the number of times each code was hit and the average value over the entire range of interest. Figure 7 shows the DNL measured with a clock frequency of 80 MHz as 116% of LSB.

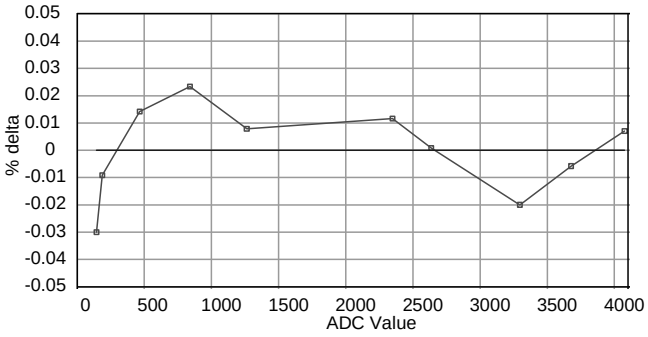

Figure 6: INL measured for an 80 MHz clock.

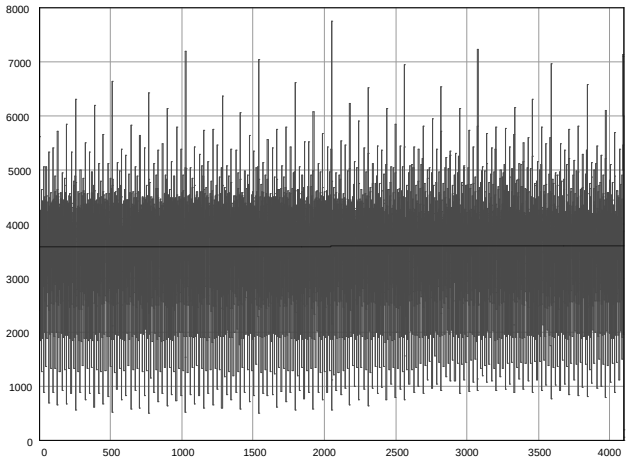

Figure 7: DNL measured for an 80 MHz clock.

E. Heap Manager

A generic Heap Manager has been developed [20, 21] for use in all PHENIX detector subsystems using analog memory for front-end signal buffering during the Level-1 trigger decision; however, due to the reduced size and power requirements for the MVD, this functional block has been partitioned such that the minimum required electronics are physically located near the detectors. The remaining circuitry resides at the ends of the detector subassembly as interface cards to the data collection modules (DCMs). Figure 8 is a block diagram of the MVD Heap Manager in context of the overall Front-End Module (FEM) showing the basic functional blocks and system partitioning.

The Heap Manager controls all on-board functions including AMU address list management and control (for asynchronous read and write operations), correlator timing, Level-1 buffering associated with trigger latency, ADC precharge/acquisition/conversion control, data handling, command interpretation/execution, and timing.

This function has been implemented using commercially available FPGAs allowing in-circuit programmability for future functional upgrades. A multi-function serial interface is used for FPGA programming, calibration setup, diagnostics and monitoring.

The beam test heap manager was implemented in two Xilinx field-programmable gate arrays (FPGA) and ran at a 10 MHz internal clock which produced a 2.5 MHz beam clock sampling frequency. The new version of the circuit is also implemented in two Xilinx FPGAs but runs as high as 63 MHz internal clock which will generate up to a 16 MHz beam clock sampling frequency, more than adequate for the 10 MHz needed by PHENIX.

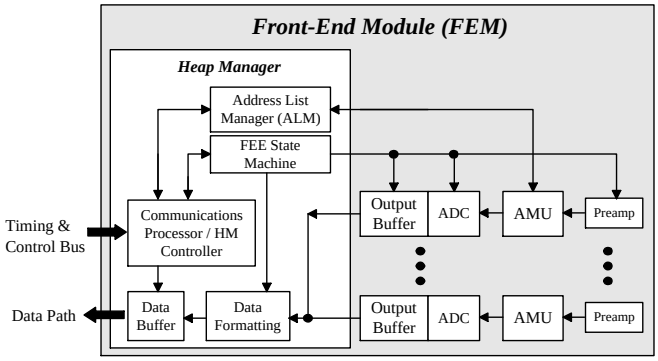

Figure 8: Front-end module including heap manager.

III. Radiation Effects

Due to the proximity of the detector to the interaction region, some significant (~10 kRad) radiation exposure is expected. The desire to utilize a standard non-radiation hardened 1.2 μm CMOS process, resulted in the need for radiation effect measurements to be performed to ensure acceptable circuit operation. Versions of the preamplifier, analog memory and ADC circuits have been irradiated to various doses of ionizing radiation. The process appears to be sufficient for doses to 75 kRad for most functions [22]. The major problem lies in the leakage current of the input protection for the preamplifier. Devices used for protection networks begin to exhibit increased leakage current due to radiation-induced decrease in the nMOS threshold voltage. A protection pad that utilizes a pMOS device for positive excursion protection and a p-implant substrate diode with channel stops for negative excursion protection was

developed. The resultant input pad leakage is now approximately that of a completely unprotected preamplifier with its associated transistor junctions. Tests with 400 keV x-rays have revealed the pad shows no degradation for a 10-20 kRad dose.

Radiation effects upon calibration and operation are not expected to be a major concern. There will be regular (every few minutes) calibration cycles to ensure the signal processing path is still functioning properly and cycles less often to ensure that the digital-analog converters (DACs) which set voltages and currents for the ADCs, discriminator thresholds, preamplifier feedback resistor values, etc., are within desired operating ranges.

IV. Beam Test Results

Each element of the front-end has been prototyped in 8-channel versions. We recently instrumented 32 channels each of two MVD silicon strip detectors, and tested them at the AGS at BNL in a secondary beam line that provided a minimum ionizing beam flux. The setup consisted of an upstream finger scintillator that covered the instrumented section of the strips, the two strip detectors, one behind the other, and a downstream coincidence paddle. The two scintillators defined the trigger. The trigger rate to strip rate ratio was about 50:1. The test setup is pictured in Figure 9.

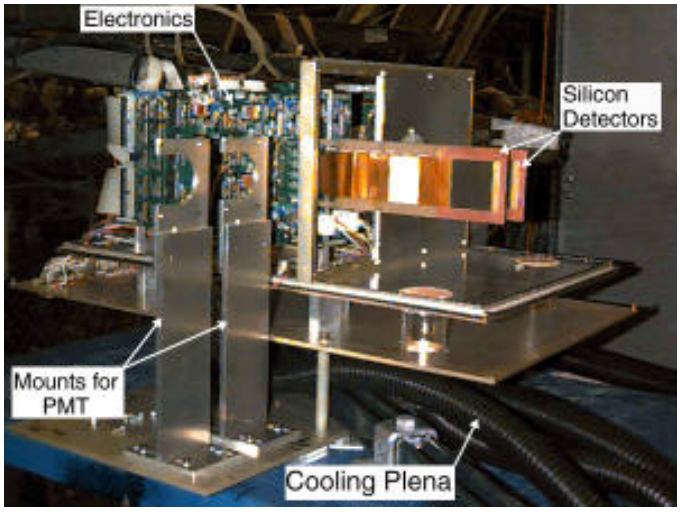

Figure 9: Beam test electronics.

The electronics die were packaged in commercial ceramic packs and interconnected on a standard G-10 printed circuit board (PCB). The silicon detectors were both outer layer types, with 7.5 cm long strips. The Kapton cable(s) connecting the strips to the readout boards was 19 cm long.

The test successfully demonstrated the operation of the entire electronics chain [23] with the exception of the analog correlator as previously mentioned. The discriminators had a threshold setting of approximately 30 mV and were functional during the beam test but could not be used for reliable triggering due to some digital noise pickup in the preamplifier. We believe the noise was due to grounding and will be further addressed in the next step of the development. We measured the signal-to-noise (S/N) on the output of the preamplifier to be about 15:1. Figure 10 shows the ADC distribution from a single silicon strip. The shape of the Landau distribution is well resolved, though the absolute separation of signal to noise is not as good as we would like. The ratio of the Landau peak to the one-sigma width of the residual noise distribution is about 6:1, whereas our goal is to achieve 10:1. Part of the noise width is due to a known problem in the version of the ADC we used for the test which had a noisy ramp. This problem has been solved in a subsequent layout. The greater noise contribution is, we feel, due to coupling of the fast clocks on the PCB into the ADC. In particular, we feel the problem is exacerbated by the long trace lengths that carry these signals.

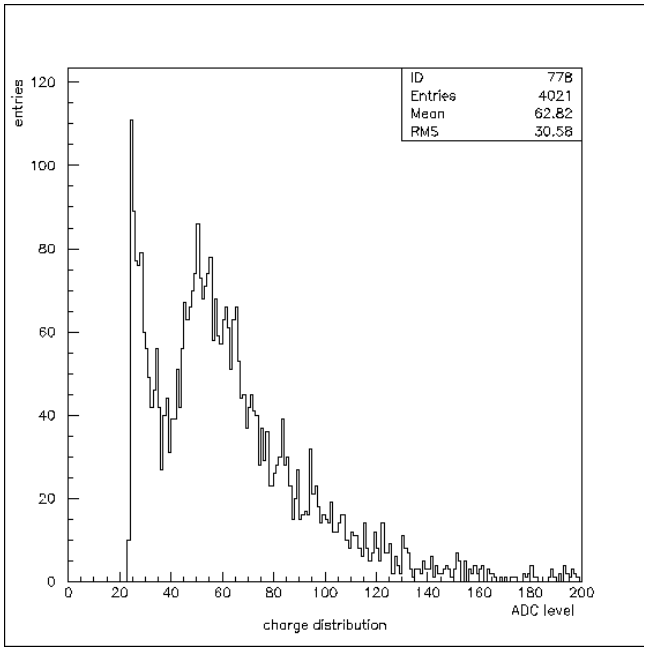

Figure 10: ADC distribution from a single silicon strip.

V. Future Work

The platform that we will use in the MVD is a multichip-module. The process we will employ is the High Density Interconnect (HDI) process. In this process, wells are milled out of an alumina substrate, and the bare die are placed into these wells so that the surface of the die are coplanar with the unmilled surface of the substrate. A polyimide layer is placed over the substrate and holes are laser drilled through the layer, directly over the die bond pads, and the contact is made by aluminization. Multiple layers are built up of trace, power and ground. We have laid out a four layer MCM. The first layer routes the analog signal traces. The second layer is a power plane split between analog and digital. The third layer routes the digital traces. The final layer is a split ground plane. The 32-channel prototype is functionally equivalent to the chain we used in the beam test, with the exception that we will use the

improved ADC. The clock traces are several times shorter than on the PCB counterpart. This fact, together with the direct contacts to the die pads, and the excellent analog to digital isolation that can be achieved in the HDI process, should significantly reduce the system noise. The MCM design is complete and ready for fabrication. It will be tested later this year.

VI. Conclusions

The circuits for the PHENIX MVD have been presented. The readout consists of preamplifier, multiplicity discriminator, analog memory, ADC and Heap Manager controller. Prototypes of the major functional blocks have been fabricated and tested and the entire system put into a beam test. The radiation tolerance of the CMOS has been tested and appears to be adequate.

VII. Acknowledgment

The authors would like to thank Norma Hensley and Teri Subich for their help in preparing this manuscript and Chen Yi Chi and Bill Sippach for their help in dielectric absorption testing.

VIII. References

[1] C. L. Britton, Jr., W. L. Bryan, M. S. Emery, M. N. Ericson, M. S. Musrock, M. L. Simpson, J. W. Walker, A. L. Wintenberg, F. Plasil, G. R. Young, M. D. Allen, L. G. Clonts, E. J. Kennedy, R. S. Smith, J. Boissevain, B. V. Jacak, J. Kapustinsky, J. Simon-Gillo, J. P. Sullivan, H. Van Hecke, and N. Xu., "Multiplicity-Vertex Detector Electronics for Heavy-Ion Detectors," *Proceedings of the First Workshop on Electronics for LHC*, Lisbon, Portugal, September 1995, pp. 84-87.

[2] I. Kipnis, H. Spieler, and T. Collins, "An Analog Front-End Bipolar Transistor Integrated Circuit for the SDC Silicon Tracker," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1994 (1095-1103).

[3] A. Adam, et al., "The Design and Construction of a Double-Sided Silicon Microvertex Detector for the L3 Experiment at CERN," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1994 (772-778).

[4] A. Seiden, "The SDC Silicon Tracker," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1994 (779-784).

[5] J. DeWitt, et al., "Signal-to-Noise in Silicon Microstrip Detectors wuth Binary Readout," IEEE Trans. Nucl. Sci., Vol. 42, No. 4, Aug. 1995 (445-450).

[6] O. Toker, et al., "Viking, A CMOS Low Noise Monolithic 128 Channel Frontend for Si-Strip Detector Readout" CERN-PPE/93-141 (1993)

[7] G. Hall, "Front End Electronics for Silicon Tracking at LHC," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1994 (1087-1090).

[8] K. Borer, et al., "APC3-A Charge Sampling, Storage, and Readout Chip for Silicon Detector Readout," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1995 (1091-1094).

[9] F. Anghinolfi, et al., "Characteristics of a 'HARP' Signal Processor with Analog Memory Operated with Segmented Silicon Detectors," IEEE Trans. Nucl. Sci., Vol. 41, No. 4, Aug. 1994 (1130-1134).

[10] J. E. Skarha., "The CDF SVX II Detector Upgrade", FERMILAB-Conf-93/302-E.

[11] B. Mours, et al., "The Design, Construction, and Performance of the ALEPH Silicon vertex Detector," CERN-PPE/96-41

[12] M. Plesko and B. Wadsworth, "Test Results for the PHOBOS-1 Preamp Chip," *MIT-LNS Electronics Facility*, Tech. Note 94-8, August 1994.

[13] R. A. Kroeger, W. N. Johnson, R. L. Kinzer, J. D. Kurfess, S. Inderhees, M. D. Allen, G. T. Alley, C. L. Britton, Jr., L. C. Clonts, M. N. Ericson, and M. L. Simpson, "Charge Sensitive Preamplifier and Pulse Shaper Using CMOS Process for Germanium Spectroscopy," IEEE Trans. Nucl. Sci., Vol. 42, No. 4, Aug. 1995 (921-924).

[14] C. Toumazou and D. G. Haigh (eds.), *Analogue IC Design: The Current-Mode Approach*, Peter Peregrinus, Ltd., London (1990), p. 300.

[15] R. Smith, et al., "A Discriminator with a Current-Sum Multiplicity Output for the PHENIX Multiplicity Vertex Detector," Presented at the 1996 Nuclear Science Symposium, Anaheim, CA, Nov. 5-8, 1996.

[16] J. W. Fattaruso, et al., "The Effect of Dielectric Relaxation on Charge-Redistribution A/D Converters," IEEE Journal of Solid-State Circuits, Vol. 25, No. 6, pp. 1550-1561.

[17 C. Y. Chi and W. Sippach, Nevis Laboratory, private communications.

[18] A. L. Wintenberg, T. C. Awes, C. L. Britton, L. G. Clonts, M. S. Emery, M. N. Ericson, F. Plasil, M. L. Simpson, J. W. Walker, G. R. Young "Monolithic Circuits for the WA98 Lead Glass Calorimeter," Proceedings of the 1994 NSS, Norfolk, VA, Oct. 30-Nov. 5, 1994, Vol. 1, pp. 493-497.

[19] M. S. Emery, et al., "A Multichannel ADC for use in the PHENIX Detector," Presented at the 1996 Nuclear Science Symposium, Anaheim, CA, Nov. 5-8, 1996.

[20] M. N. Ericson, M. S. Musrock, C. L. Britton, Jr., J. W. Walker, A. L. Wintenberg, G. R. Young, and M. D. Allen, A Flexible Analog Memory Address List Manager for PHENIX," IEEE Trans. Nucl. Sci., Vol. 43, No. 3, June 1996 (1629-1633).

[21] M.N. Ericson, "Development of a Front-End Controller/Heap Manager for PHENIX," Presented at the 1996 Nuclear Science Symposium, Anaheim, CA, Nov. 5-8, 1996.

[22] C. L. Britton, Jr., A. L. Wintenberg, G. R. Young, T. C. Awes, M. Womac, E. J. Kennedy, R. S. Smith, "Post-Radiation Memory Correction Using Differential Subtraction for PHENIX," IEEE Trans. Nucl. Sci., Vol. 43, No. 3, June 1996 (1564-1569).

[23] J. S. Kapustinsky et al., "A Multiplicity Vertex Detector for the PHENIX Experiment at RHIC," submitted to proceedings of the 4th International Conference on Position Sensitive Detectors, Manchester, UK, Sept. 9-13, 1996.