Heavy Quarks LDRD Data Acquisition System

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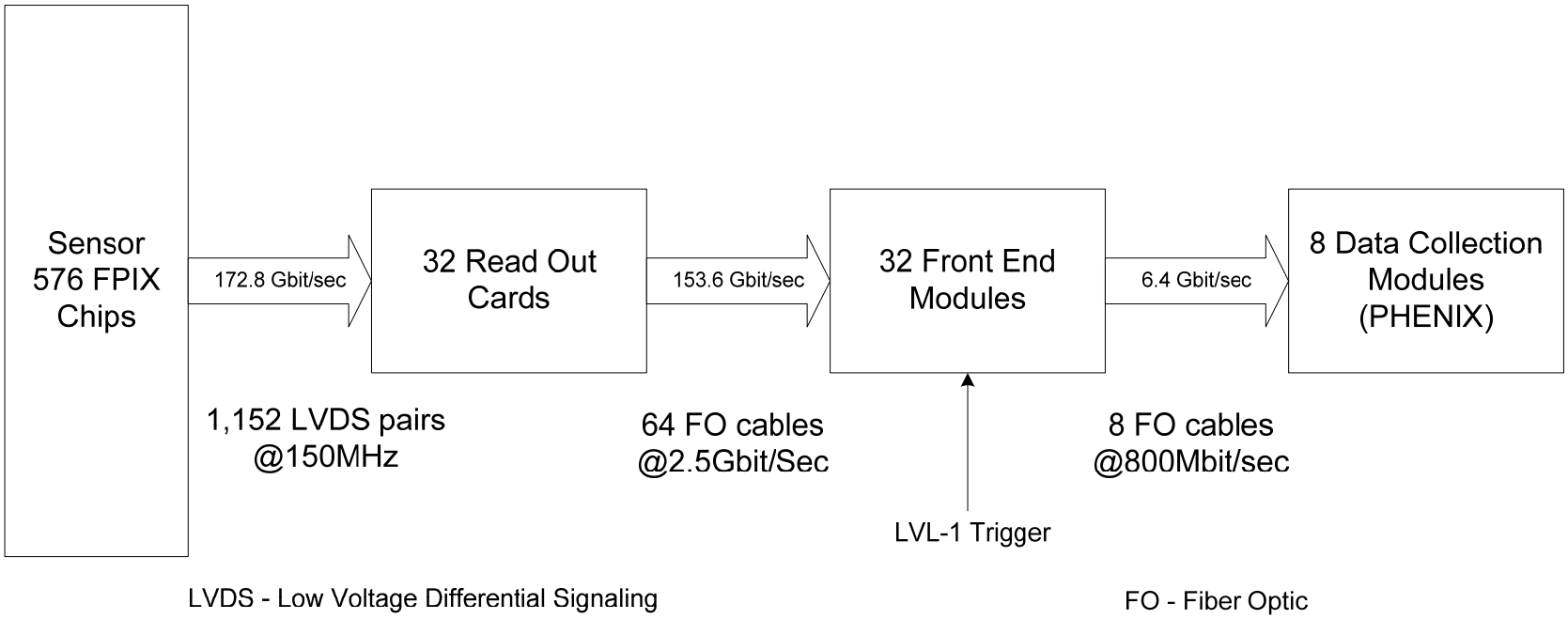
Introduction

- Requirements
- Solution
- System Overview
- Concluding Remarks

Requirements

- Timing
  - Triggering
    - Test algorithm
  - Data Collection Module (DCM)
    - Buffer data for 6.4 us
    - Transfer data to DCM within 40 us
- Radiation
  - Tolerance for IR environment (<10kRad)
  - 1.0×10^{-7} to 1.6×10^{-5} /bit/hour upset rates
- Mechanical
  - Fits within envelope
- PHENIX Environment
  - Noise
  - Magnetic Fields
  - Interference

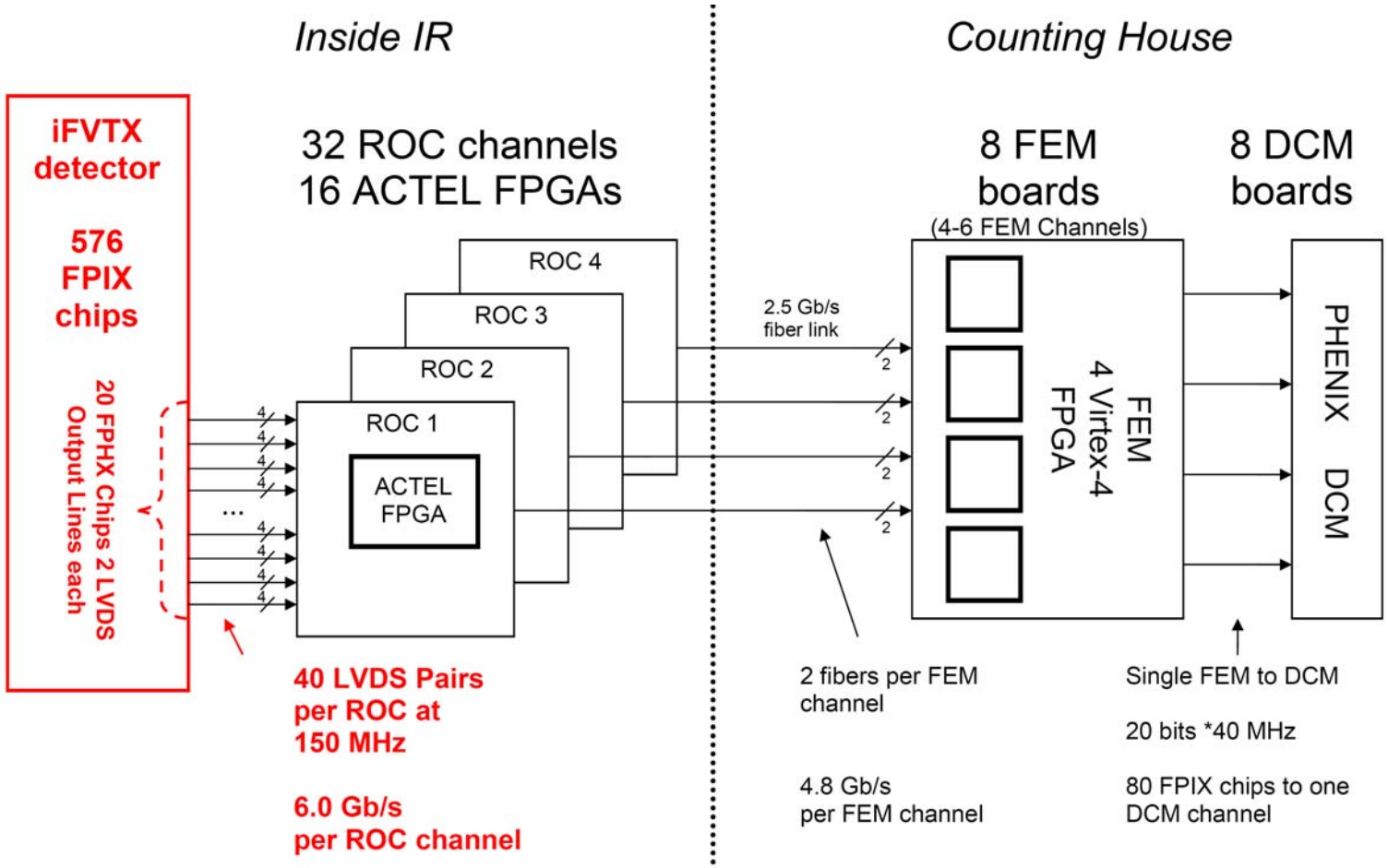
iFVTX DAQ System: Functional Block Diagram



Solution

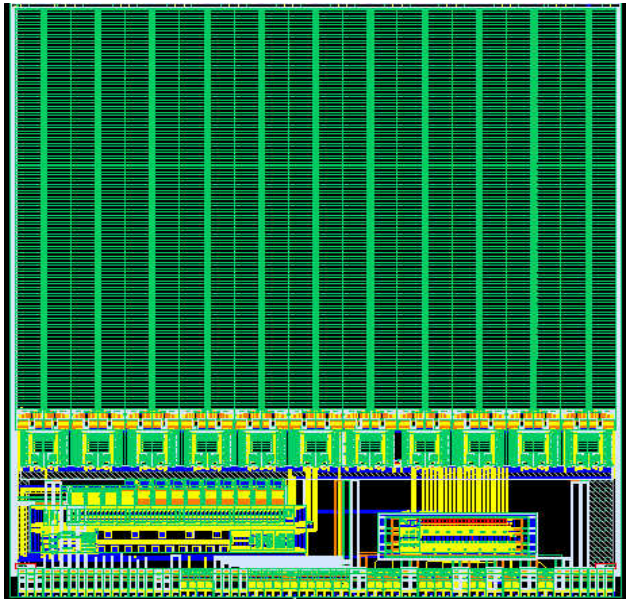
- Two Part Readout Electronics
  - Interaction Region (IR) Electronics: Read Out Card (ROC)
    - Radiation Tolerant
    - Data Rate Reduction
    - Fiber Optic Output
  - Counting House Electronics: Front End Module (FEM)
    - Data Buffering
    - Data Formatting
    - Triggered Readout
- PHENIX DAQ
  - Combine packets into event
  - Event Building

iFVTX DAQ System - FPIX



FPIX Chip

- Data push readout
- Zero suppression
- Two LVDS readout lines at 150 MHz for 300 Mbits/sec data rate



b_{23}	b_{22}	b_{21}	b_{20}	b_{19}	b_{18}	b_{17}	b_{16}	b_{15}	b_{14}	0	0	0	0	0	0	0	0	0	0	0	0	0	1

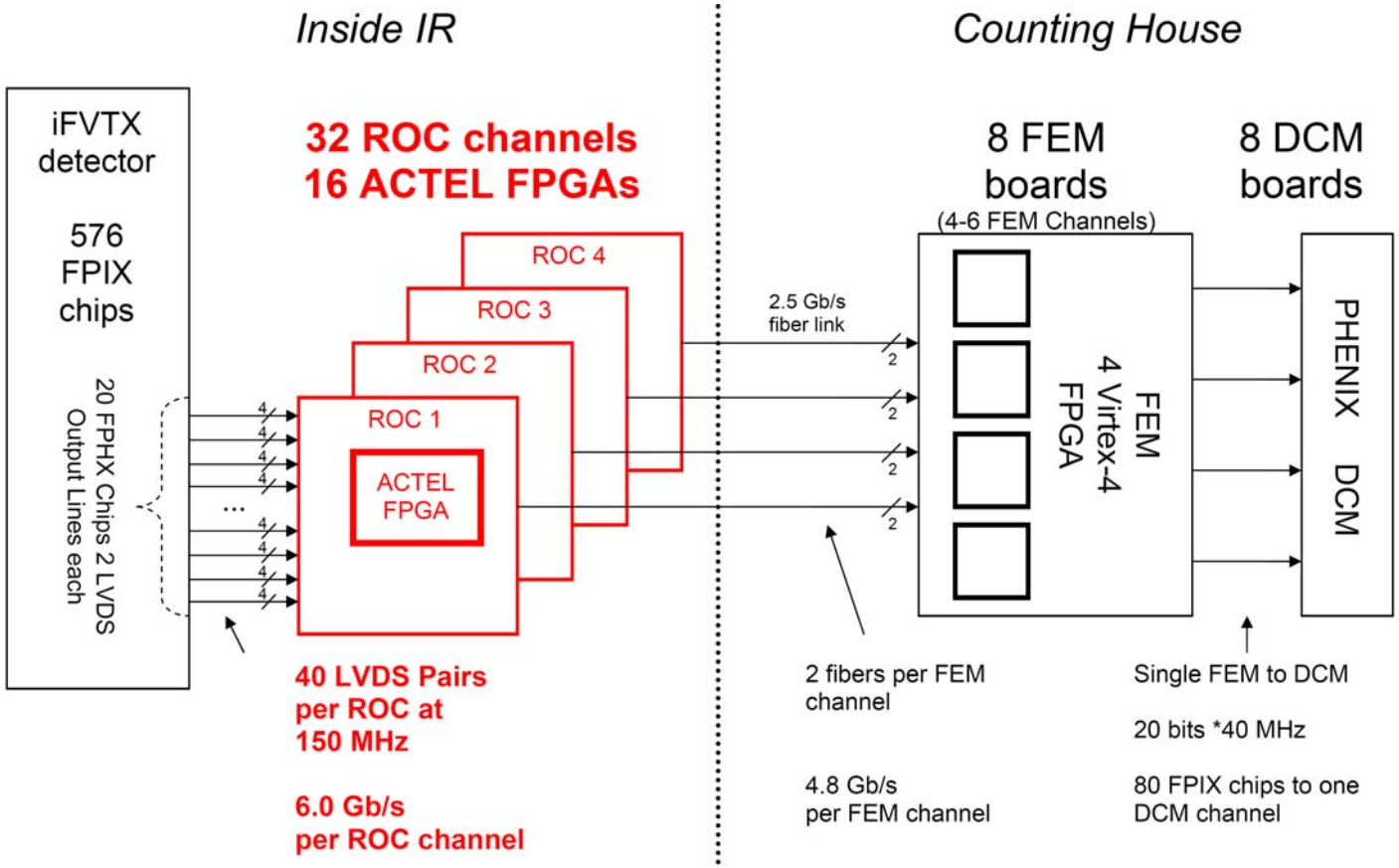
Status Sync Word Mark

b_{23}	b_{22}	b_{21}	b_{20}	b_{19}	b_{18}	b_{17}	b_{16}	b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_{09}	b_{08}	b_{07}	b_{06}	b_{05}	b_{04}	b_{03}	b_{02}	b_{01}	1

Row Number Column BCO ADC Word Mark

BCO – Beam Counter

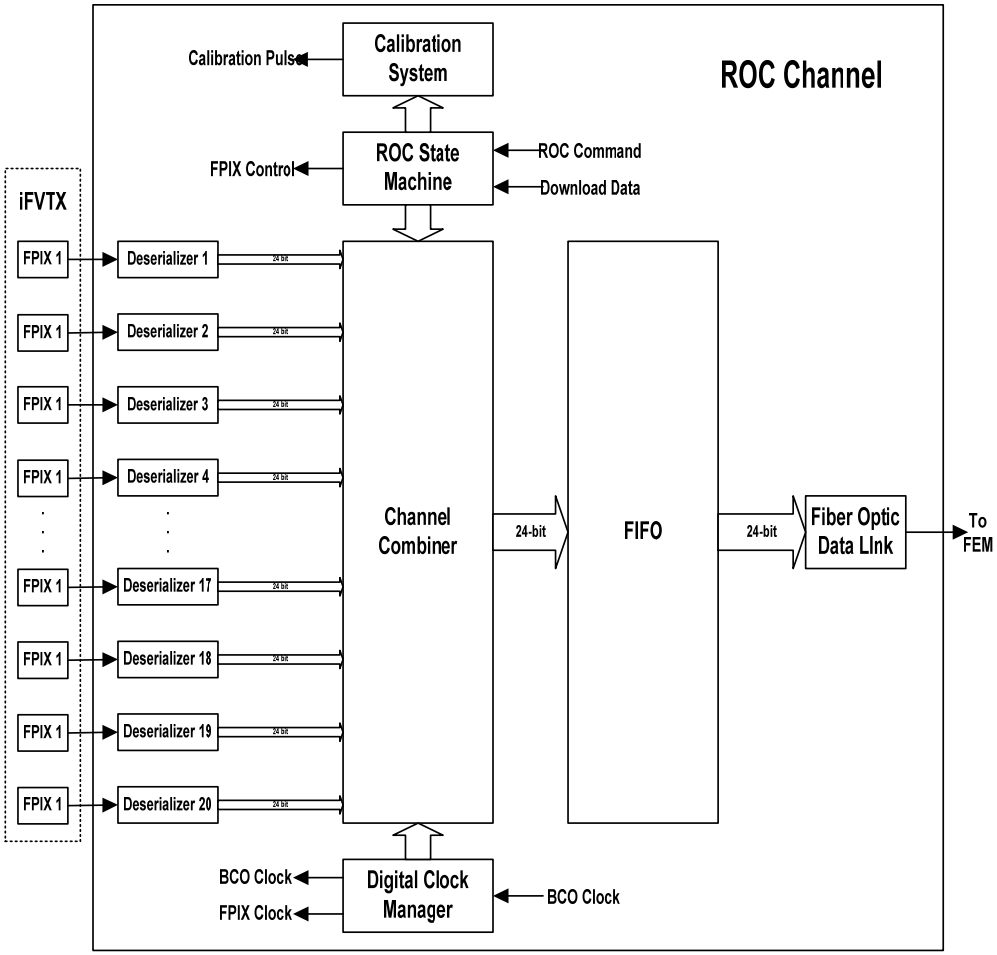
iFVTX DAQ System – Read Out Card



Read Out Card Features

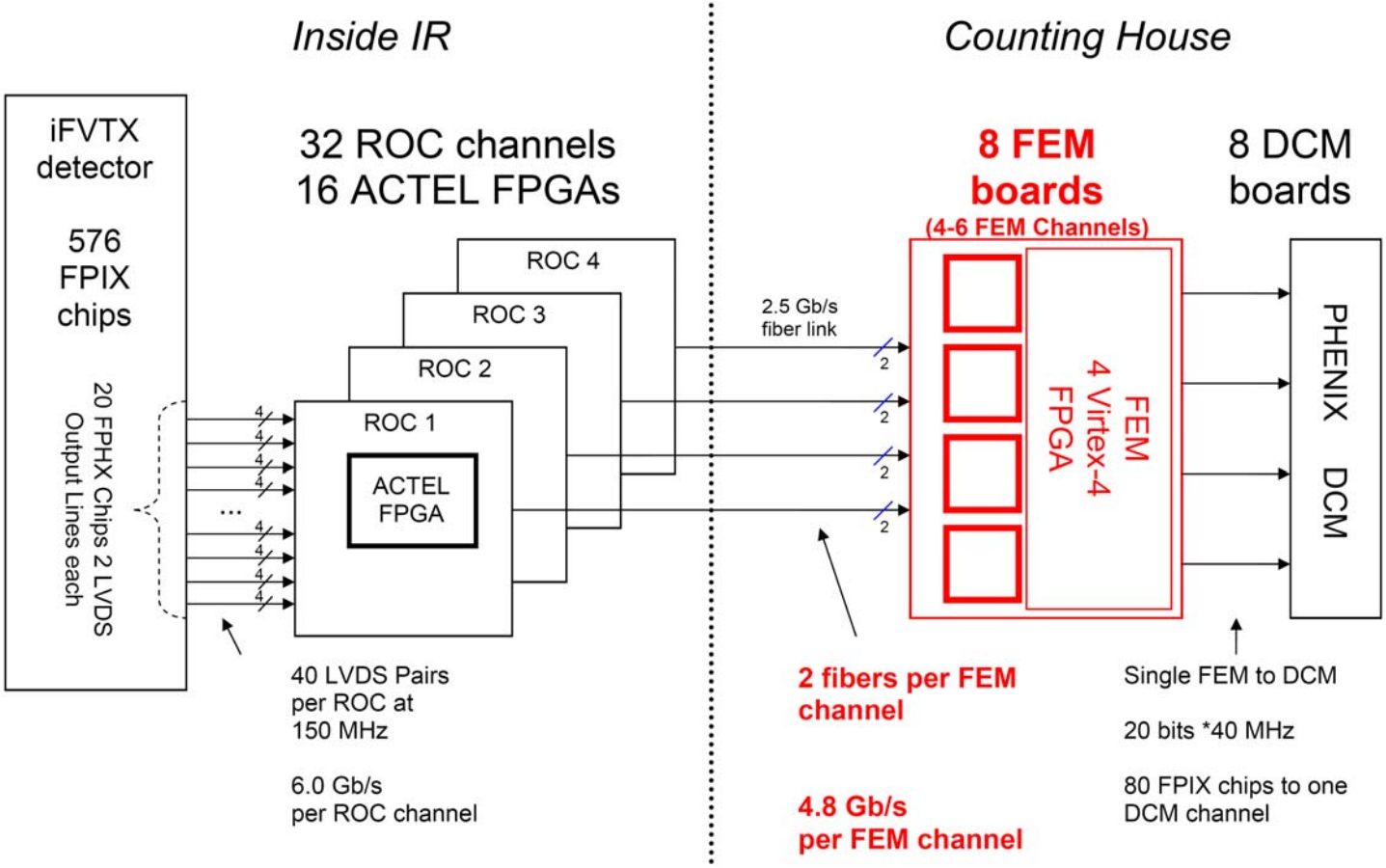
- Radiation tolerant Field Programmable Gate Array (FPGA) and Serializer/Deserializer (SERDES)
- Radiation Tolerance >20kRad
- Data Combined from 20 FPIX chips into each ROC
- Data Synchronization
- Data Compression

ROC Prototype



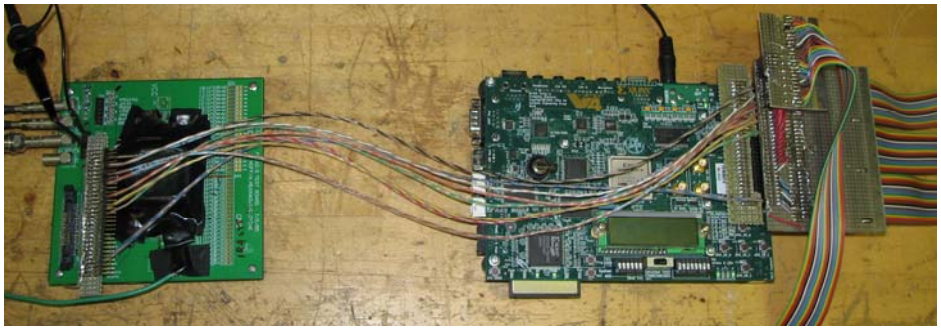
ROC Block Diagram

iFVTX DAQ System – Front End Module

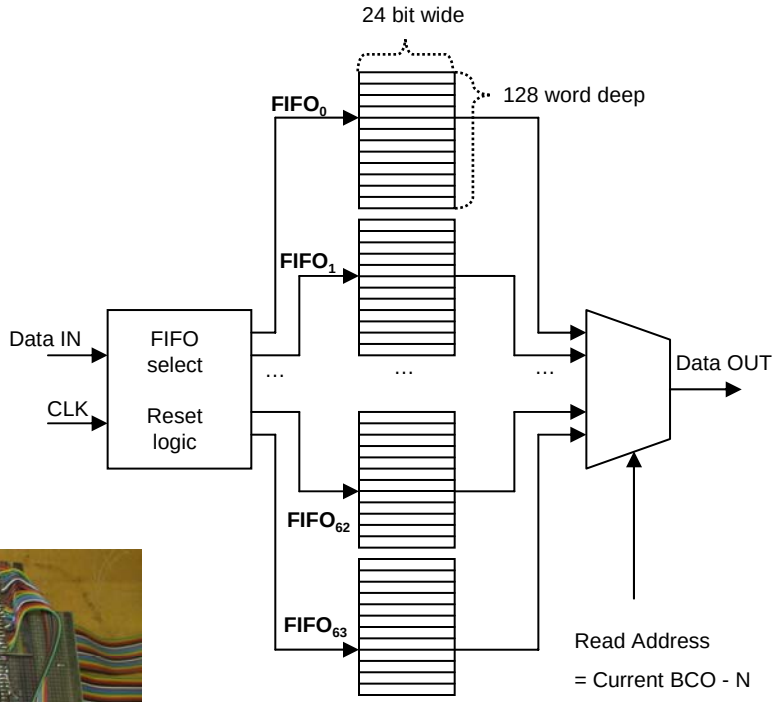


Front End Module Features

- Store data by BCO clock and buffer for 64 BCO clocks
- Read upon LVL-1 request
- VME standard form factor
- Xilinx FPGA
- 4 FEMs per VME card

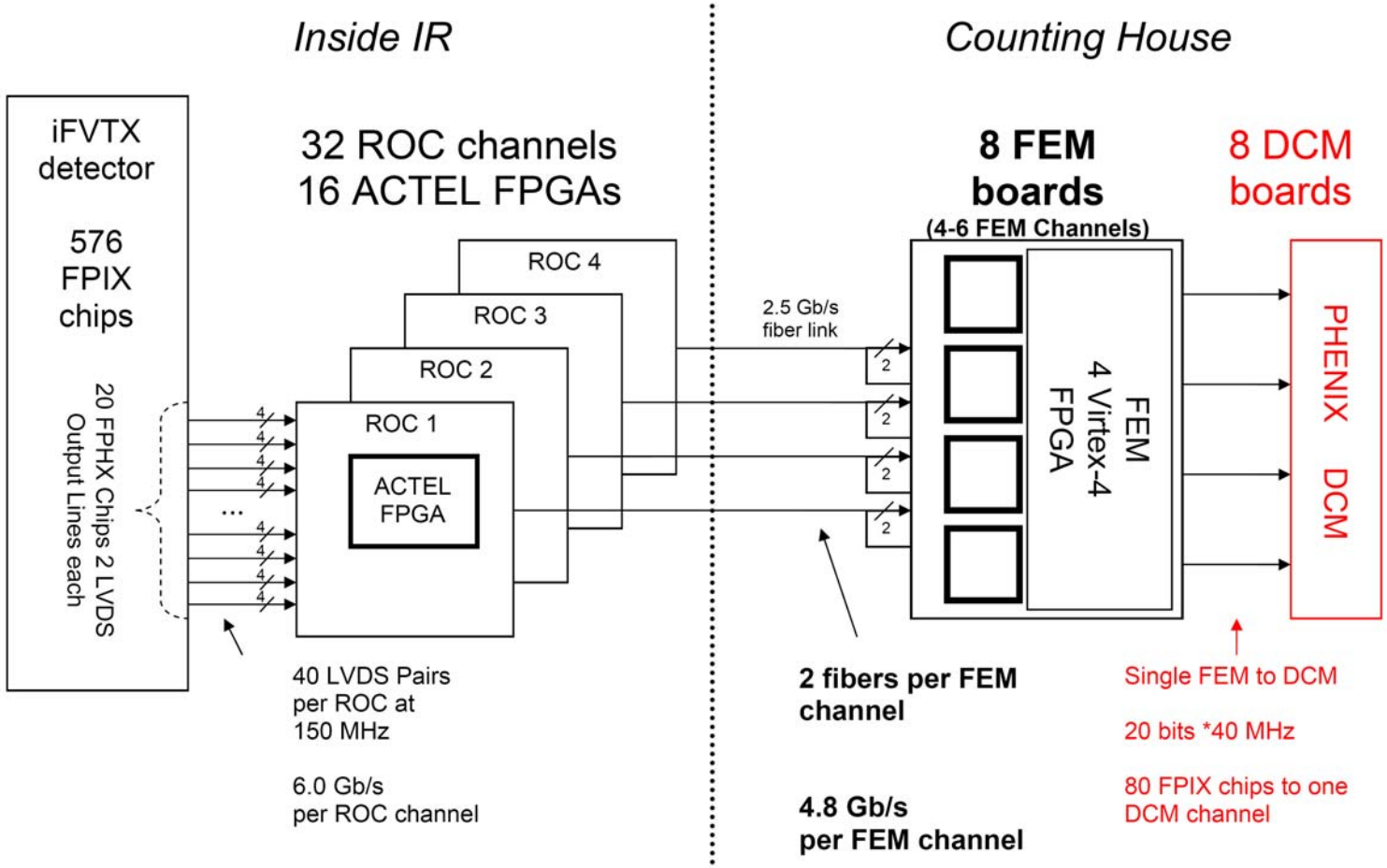


FEM Prototype



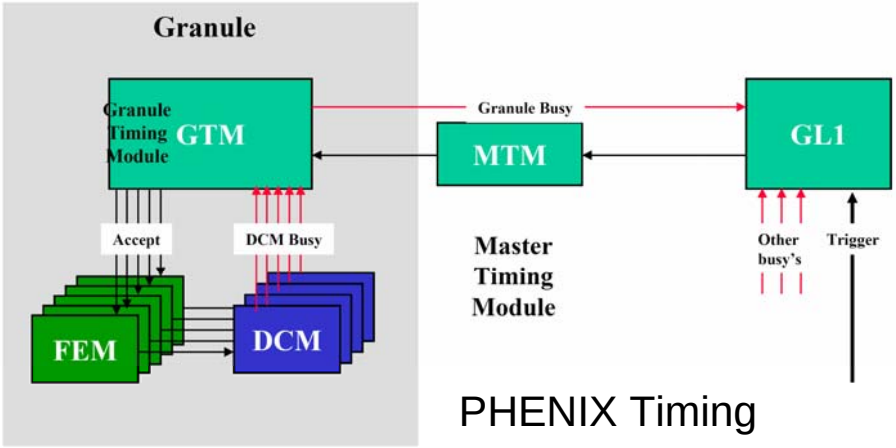
FEM Block Diagram

iFVTX DAQ System – PHENIX DCM

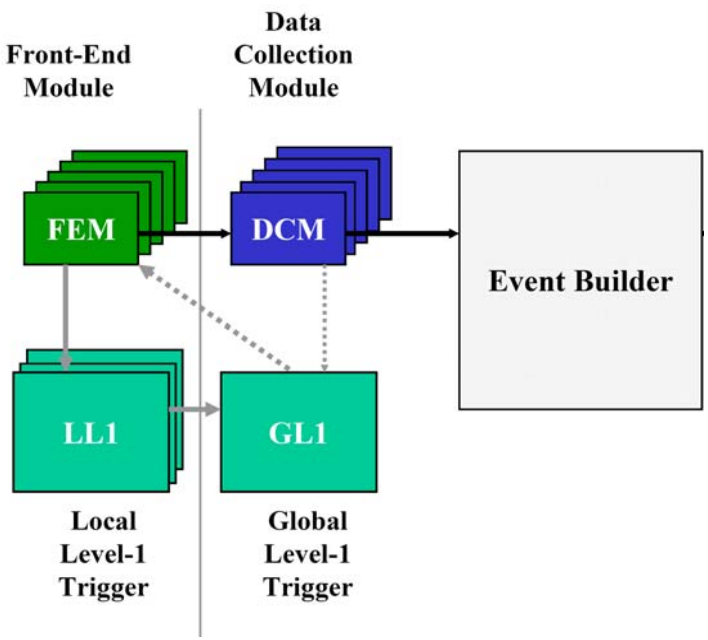


PHENIX Data Acquistion System

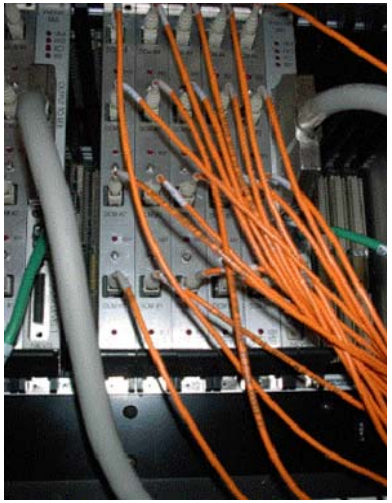
- Standard PHENIX protocol
- No Modifications needed



PHENIX Timing



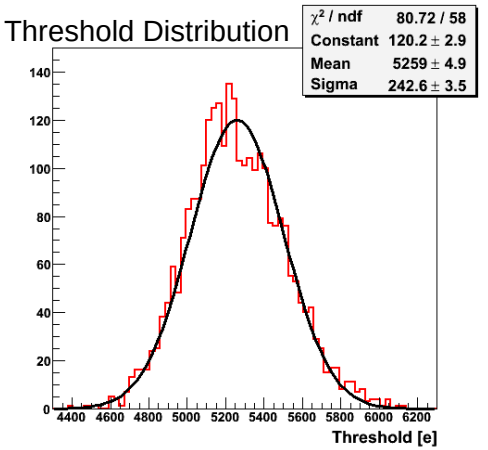
PHENIX Triggering

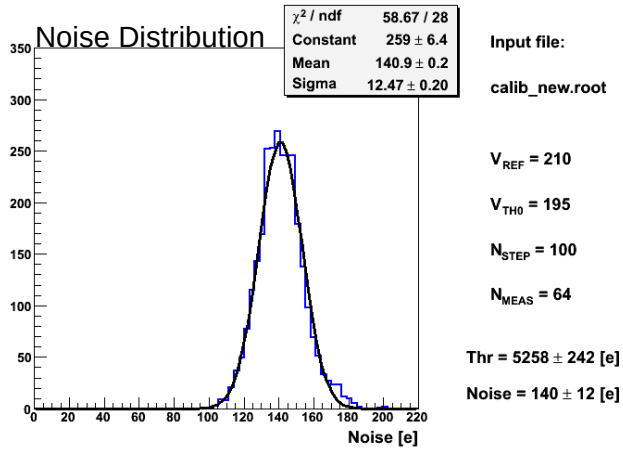


PHENIX
DCM Crate

System Performance Results

- Realistic triggered full-speed readout
- No data loss
- Results of threshold scan confirm FNAL test results
- The proposed readout design is working as expected





Input file:

calib_new.root

V_{REF} = 210

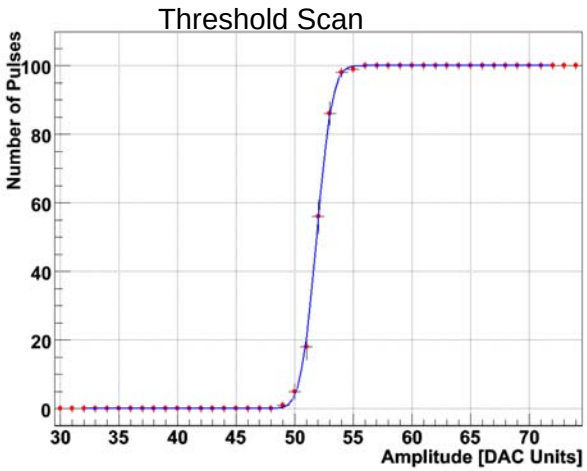
V_{TH0} = 195

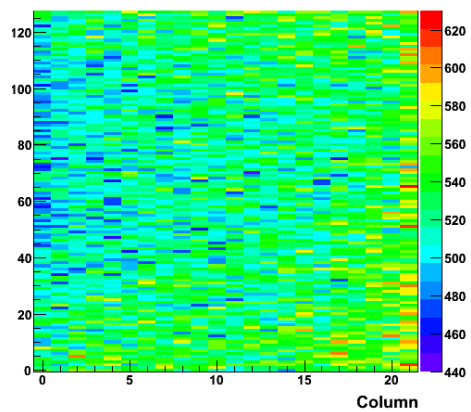
N_{STEP} = 100

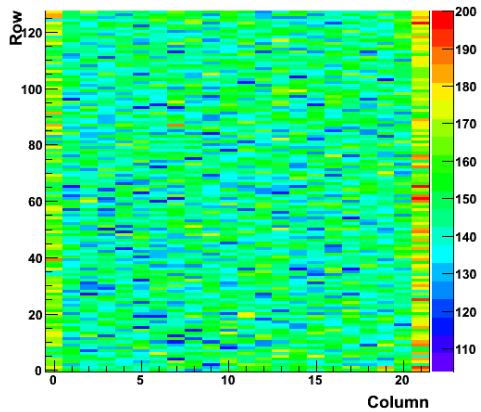
N_{MEAS} = 64

Thr = 5258 ± 242 [e]

Noise = 140 ± 12 [e]

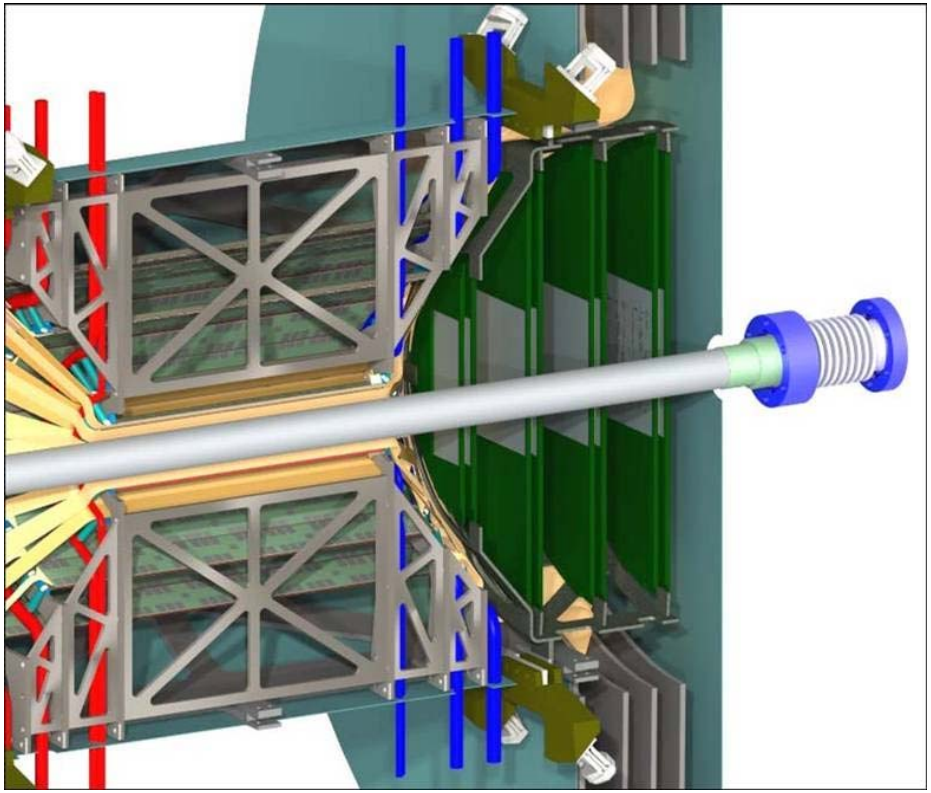


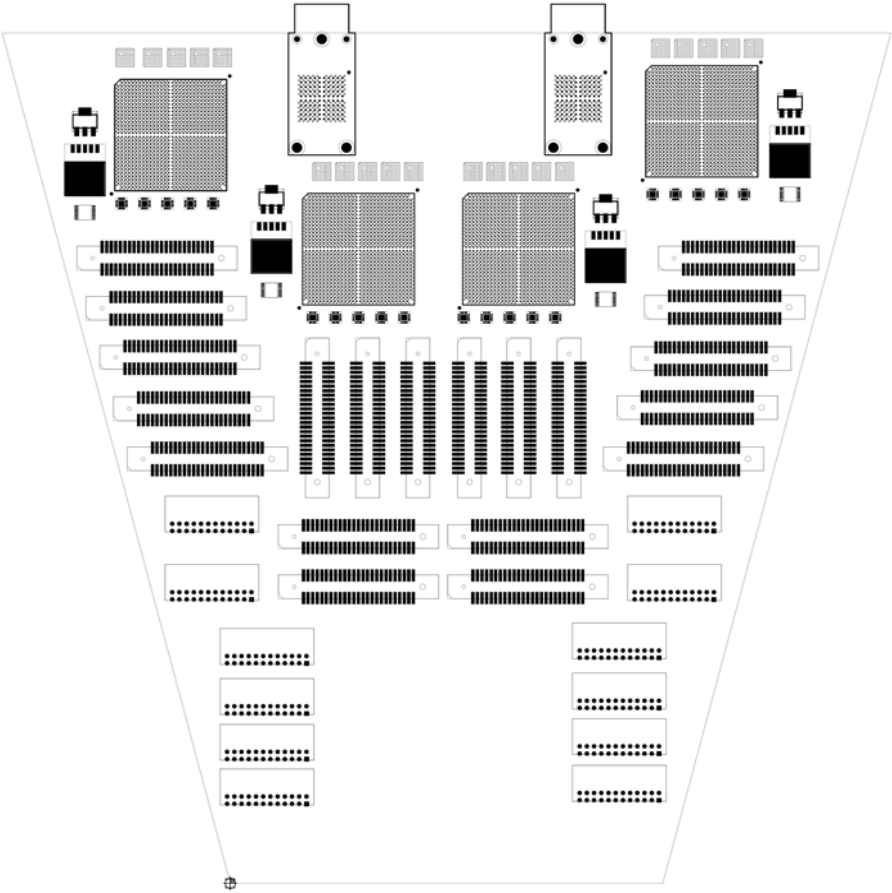




0 dead pixel:

Integrated System





LDRD ROC Concept PCB

Current Status

- Demonstrated ROC and FEM functionality with evaluation boards
- Demonstrated system functionality at full speed
- System data collection requirements analyzed: Triggering and DCM requirements met
- No critical R&D issues for electronics hardware

Next Steps

- Demonstrate 2.5 Gbit/sec FO Link (June 02)
- Full up Prototype ROC, FEM and FO communications including integration with PHENIX data collection system (DCM) (October 07)
- Start engineering systems electronics and interconnections for Noise, EMI and Grounding requirements (October 07)
- DAQ Electronics production complete (Mar 08)